

JUNE 28, 1984

**BOOM SLOWS CAPTIVE CHIP MAKERS ON WAY TO MERCHANT MARKET/89**

Concurrent C eases programming of real-time multiprocessing systems/125

Advanced bipolar process squeezes more out of VLSI/131

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International

# Electronics®

SPECIAL  
REPORT

## COMPUTER GRAPHICS





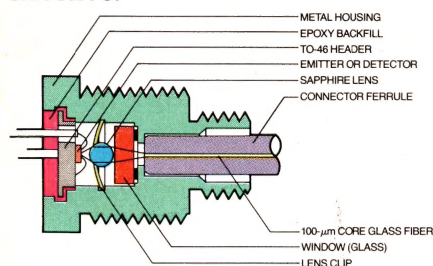
# Design in leadership with fiber optic components from HP

## Depend on our commitment to fiber optic technology.

Today, fiber optics is a leading technology for data transmission because it's faster, more reliable, more secure and often less expensive than alternative technologies.

Hewlett-Packard's commitment to fiber optic technology began ten years ago. Since then, we've applied these years of experience in LED emitters, detectors, integrated circuits, optical fiber and packaging to make HP your best choice for fiber optic components.

Our wide range of fiber optic components gives you performance choices that are reliable, easy-to-use and cost-effective.



*This cross section of an HP fiber optic transmitter shows HP's advanced lensing scheme for optimal coupling of light into the fiber.*



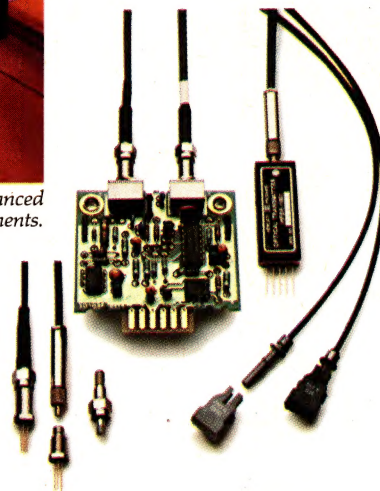
*At Hewlett-Packard's Optical Communications Division, engineers use advanced research and development equipment to test state-of-the-art fiber optic components.*

## Choose from three families of products.

There are currently three families of HP fiber optic products: Plastic Snap-In Components; Miniature Link Components; and High Performance Modules. The families are growing, too. New products will offer increasingly faster data rates and greater distances. Packaging developments and improved manufacturing techniques will keep costs coming down.

Start moving your data today with HP fiber optics and get the added assurance that your designs will keep you a leader tomorrow. HP's worldwide team of applications and sales engineers is ready to help you.

To learn more about HP fiber optics, circle the reader service number below. For pricing and delivery information, contact your local HP Authorized Components Distributor. In the U.S., call Hall-Mark, Hamilton/Avnet, Pioneer Standard, Schweber, or the Wyle Distribution Group. In Canada, call Hamilton/Avnet or Zentronics, Ltd.



**HP: The right choices for moving data today and tomorrow.**





Cover photograph by Walter Chrynwski



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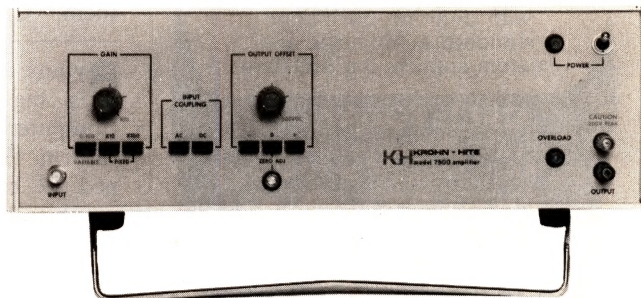
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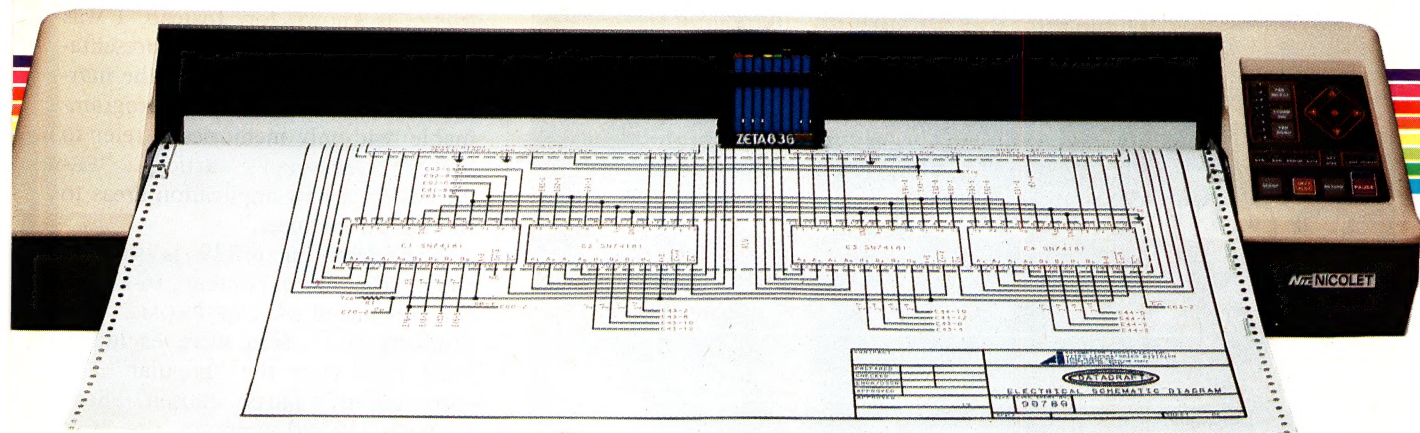
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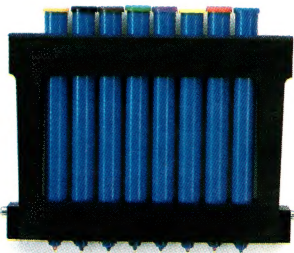


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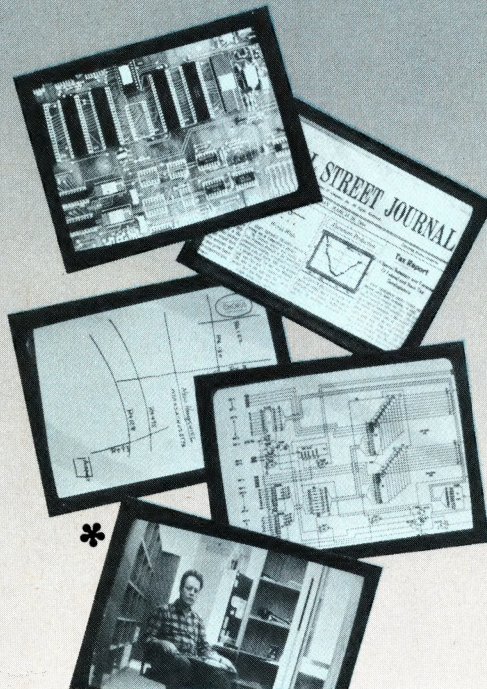
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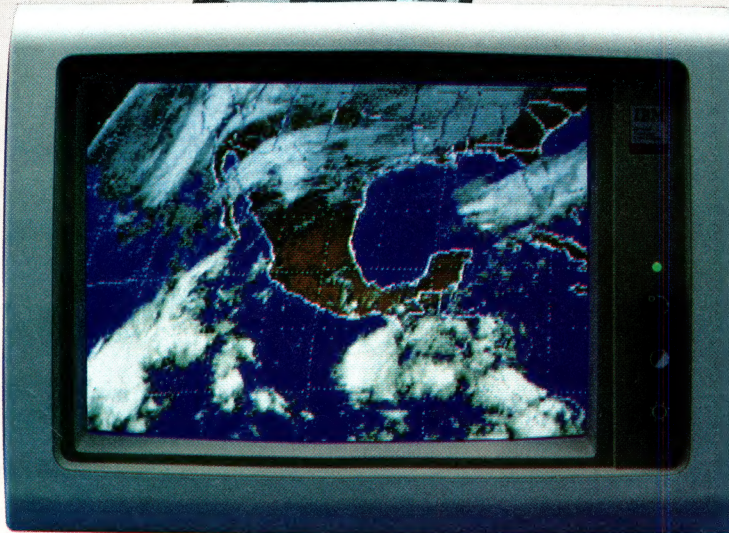
**Input Channels:** Four video plus external trigger

**I/O Slots:** 1 IBM PC or PC/XT compatible

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We offer a selection of cameras, accessory kits, and compatible graphic adaptors. For our price/catalog and further details, write,

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\*The B&W pictures are taken with a 35mm SLR camera. The pictures were captured with an RCA TC 1005 video camera on an IBM XT and sent to the monitor with a Tecmar Graphics Master™ graphics adapter in the 640 x 400 x 16 level mode via its composite output.

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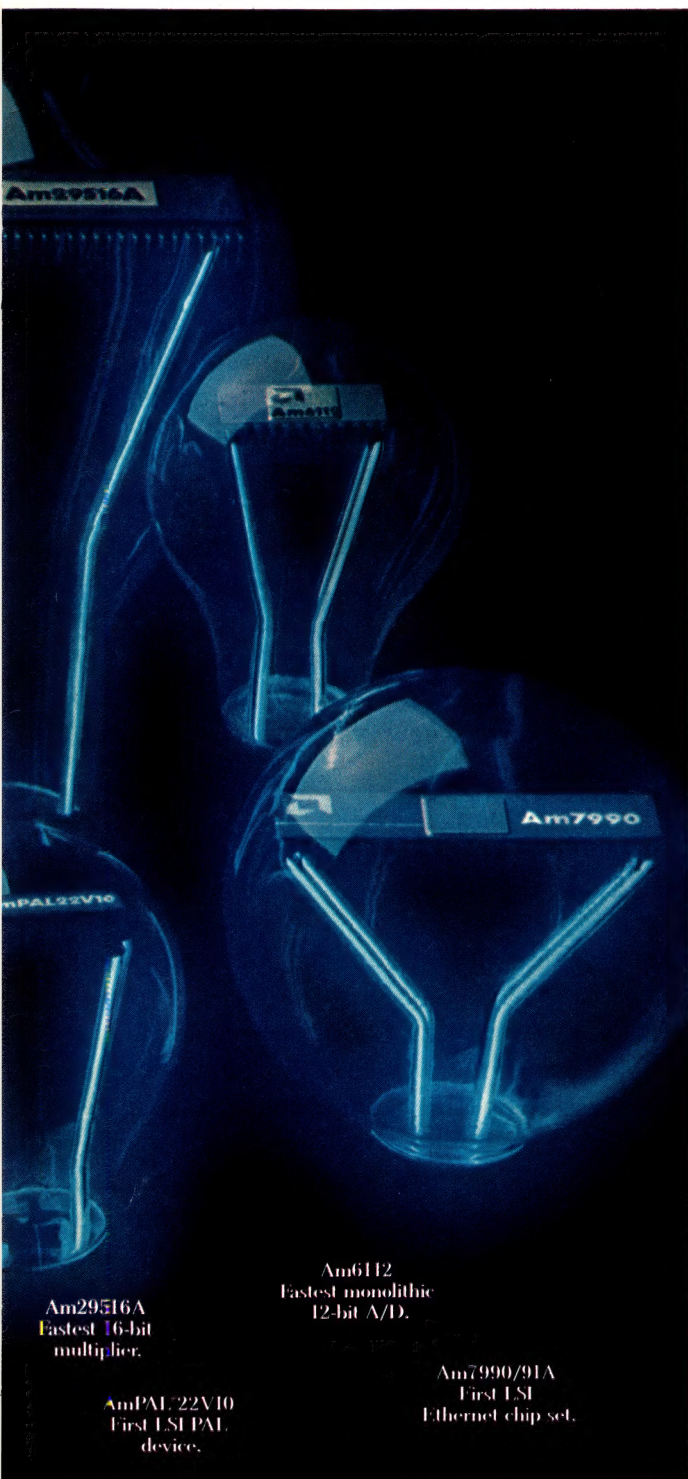
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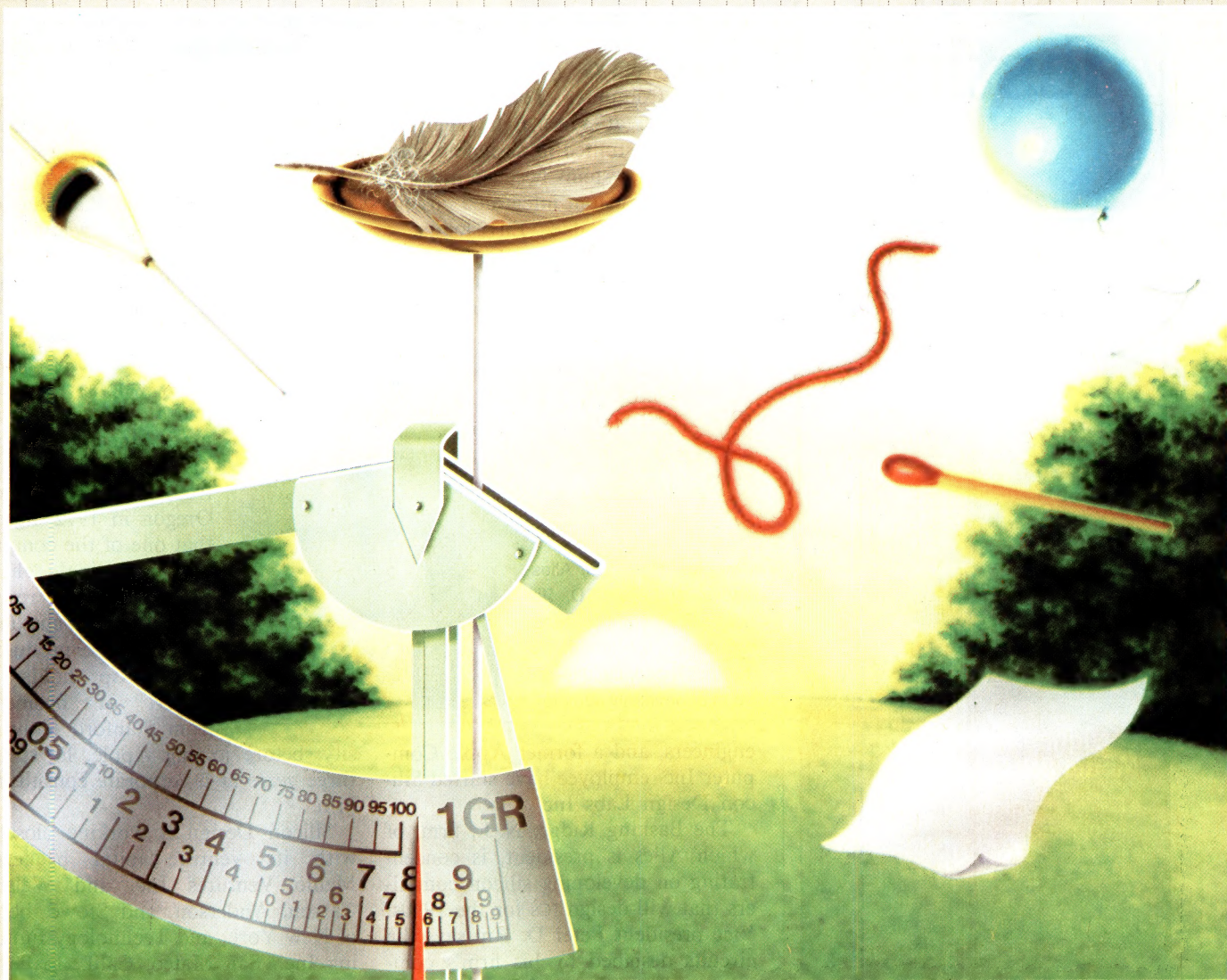
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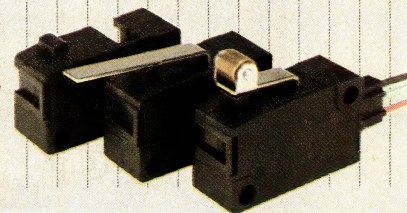
Feather light operating forces of as little as 1 gram allow our new solid state VX series to open up all kinds of switching possibilities.

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Find out more about these new low-force switches from Honeywell Europe SA, Avenue Henri Matisse 14, B-1140 Brussels, Belgium.



**Together, we can find the answers.**

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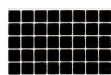
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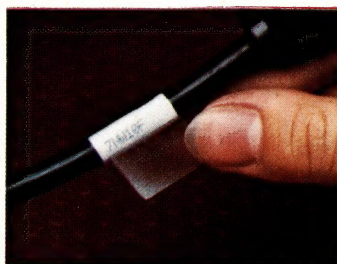
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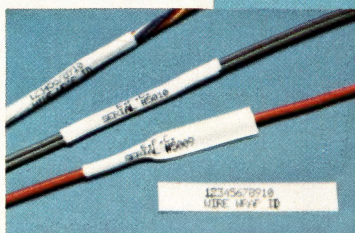
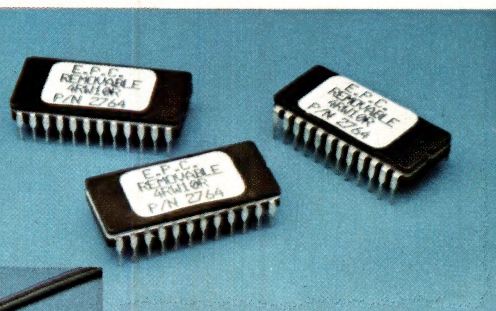
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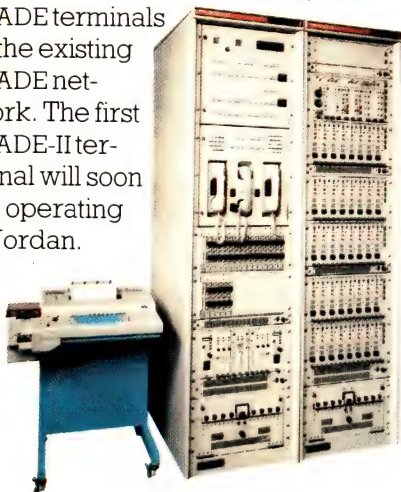
## NUMBER 130

### SPADE-II FOR INTELSAT ATLANTIC REGION

**S**PADE-II terminal equipment, designed to the latest INTELSAT SPADE Specification and completely compatible with existing SPADE terminals, will soon make its operational debut in the INTELSAT system, Atlantic Ocean Region. Incorporating state-of-the-art micro-processors and LSIs, it provides excellent reliability as well as simple operation.

The SPADE system allows a user to establish a communications circuit on demand with any other SPADE user, greatly improving satellite transponder utilization efficiency. It handles several times more telephone traffic using the same number of SCPC channel units. In addition, it considerably reduces annual operation cost because each SPADE circuit is billed not on a fixed annual rate but on an actual utilization basis.

NEC supplied 28 of the original SPADE terminals in the existing SPADE network. The first SPADE-II terminal will soon be operating in Jordan.



### NEW LDR SYSTEM FOR BUSINESS COMMUNICATIONS

**N**EC now offers a highly sophisticated 10.5GHz digital local distribution radio (LDR) system. It meets the increasing need for low-cost, high-speed, and quality transmission of digital data for business communications.

NEC's 10.5GHz system, first put into operation in New York City, was developed as an advanced technological solution to local distribution problems. The system is based on a field-proven 2GHz LDR system using TDMA technology.

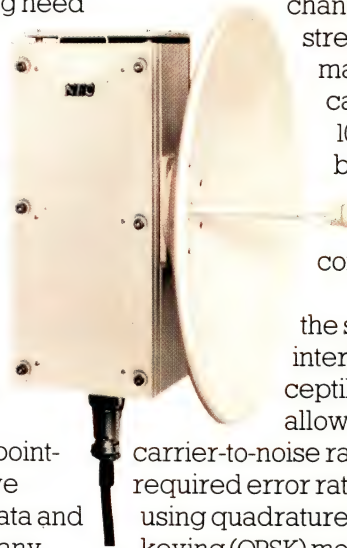
The new system provides point-to-multipoint digital microwave links for local distribution of data and voice from a node station to many subscribers with a single pair of radio frequencies. Each system

covers a 90-degree sector with a radius of up to 15km. As many as 26 subscriber stations in each sector are served by one local node station. Radio frequency reuse in several quadrants can significantly increase the service range and maximize system flexibility.

The LDR system transmits up to twenty-six 56 or 64 kbps data or voice channels—a total bit stream of approximately 1.8Mbps per carrier. As many as 104 subscribers can be accommodated by one node with a maximum configuration.

A key feature of the system is its low interference susceptibility. The system allows a very low

carrier-to-noise ratio to obtain the required error rate performance by using quadrature phase shift keying (QPSK) modulation, thus enabling many frequencies (up to 20) to be used in the same area.



### NEW 1,300nm LASER DIODES

**N**EC's new laser diodes feature our exclusive Double-Channel Planar Buried Heterostructure (DC-PBH). This feature improves efficiency and reduces the temperature dependence of the operating current. Double channel structure also minimizes crystalline defects to provide more stable operation.

As a result, new laser diodes guarantee 5mW minimum output up

to 60°C. They eliminate the need for thermo electric coolers and thus permit more compact equipment design. They also feature low threshold and operating currents: 20mA/50mA(25°C, 8mW).

The improved service life results in an estimated MTTF of more than 100,000 hours for 5mW operation at 50°C. Other features include stable fundamental transverse mode and nearly circular beam.

**NEC**  
NEC Corporation  
Tokyo, Japan.



# Instruments line driver drives Data to market faster.

cation, providing fault protection and power up/power down protection, as well as enable and fault flags.

## Performance as specified

Control Data engineers learned about the '174 early on. Moving quickly, they evaluated and designed it in, counting on it to perform to very exacting specifications. It did . . . perfectly.

## The alternative? Greater costs

Control Data engineers estimate that a discrete-component alternative would have resulted in at least a 15% increase in board area to accommodate the necessary additional components.

As it turned out, the SN75174 driver contributed important system savings to the design, improved reliability, helped Control Data get to market faster. ■

The SN75177A is active high and the SN75178A is active low. This allows you to pair the two back-to-back for improved bidirectional communication when extending cable distance.

## SN75172/SN75174

### Quad Drivers,

### SN75173/SN75175

### Quad Receivers

The two quad drivers operate from a single +5 V supply, yet maintain a high-impedance output over a common-mode range from -7 V to +12 V with power on or off. Without sacrificing speed. Both drivers have maximum delay times of 50 ns, rise and fall times of less than 80 ns. They allow data rates up to four megabaud.

The major difference between the two drivers is the enable scheme. And this increases design flexibility. All four drivers in the SN75172 are enabled at once, whereas they are enabled in pairs in the SN75174.

The two quad receivers are similar to existing RS-422 devices but have higher input impedance and extended common-mode range, from  $\pm 7$  V to  $\pm 12$  V. Sensitivity is  $\pm 200$  mV over -12 V to +12 V common-mode range.

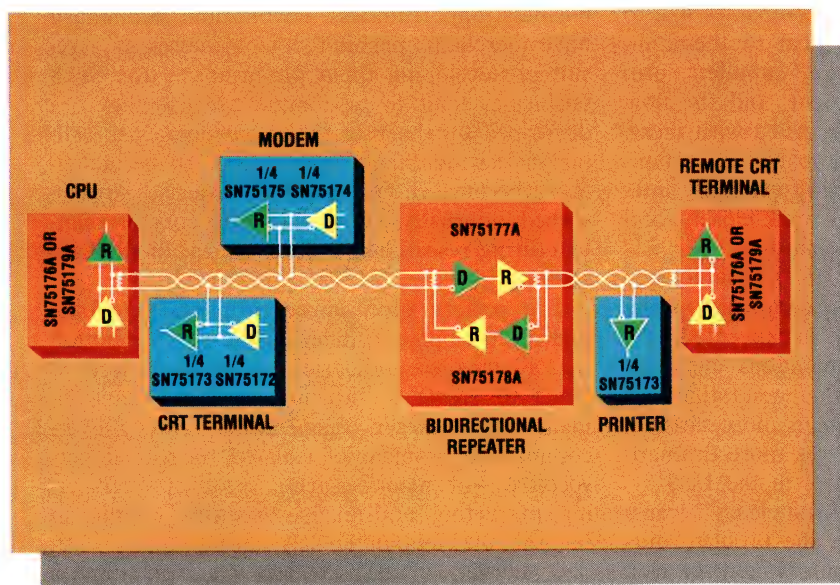
## All other standards covered, too

In addition to offering these new devices that meet RS-422 and other party-line applications, TI offers the industry-standard ICs you need to meet the EIA RS-485, RS-232-C, and RS-423 standards, as well as IEEE 488.

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## SN75177A/SN75178A

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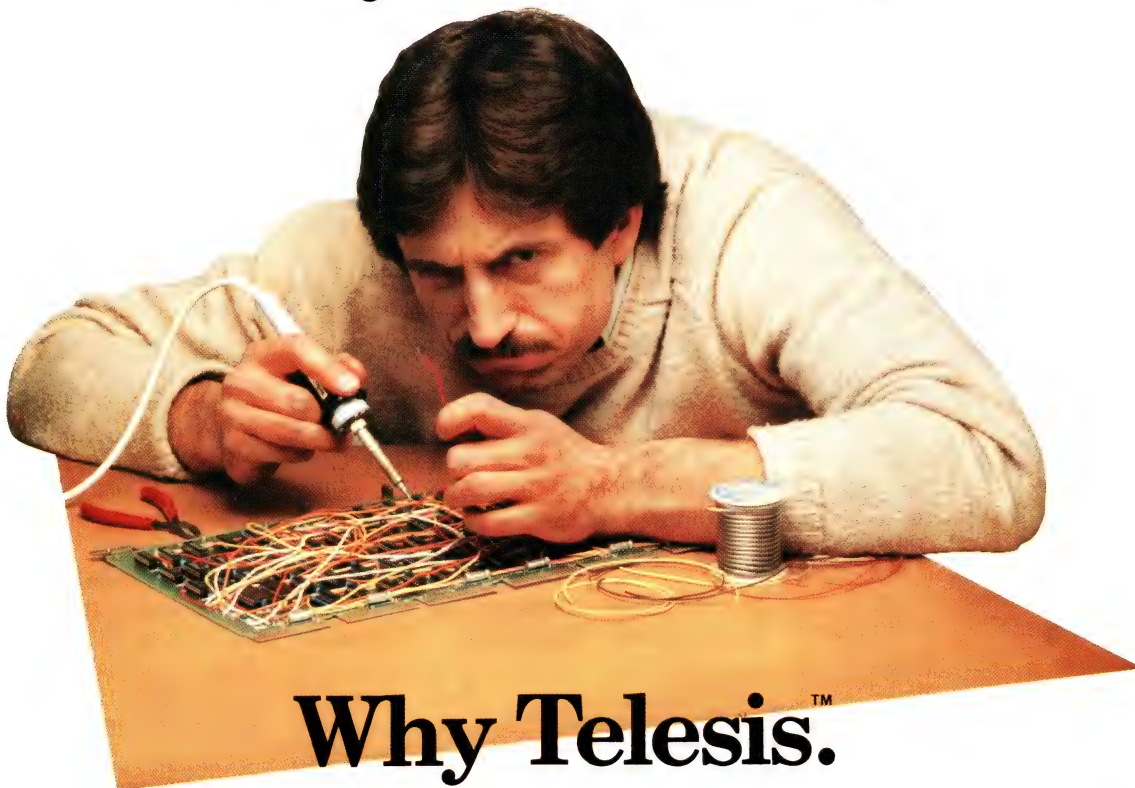
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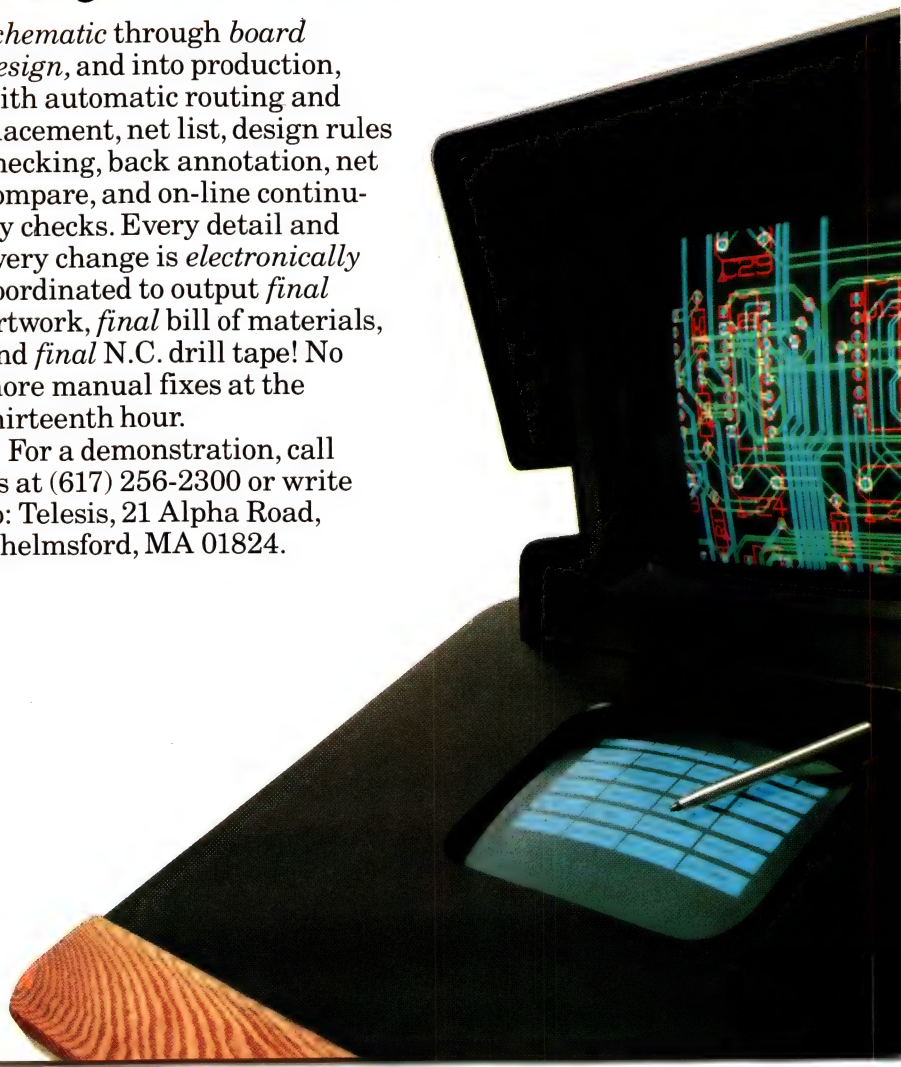
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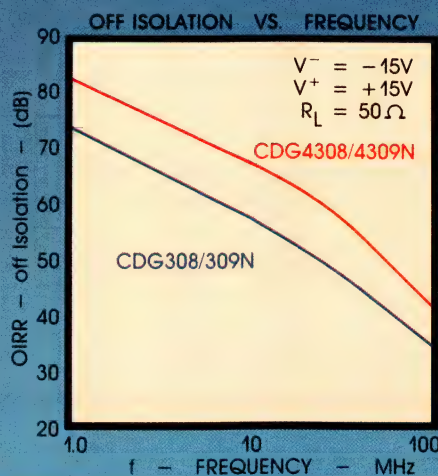
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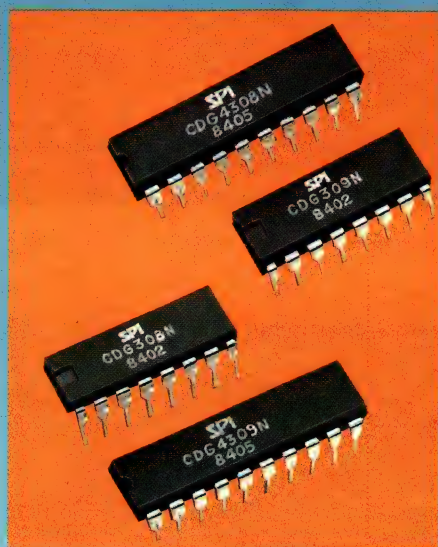


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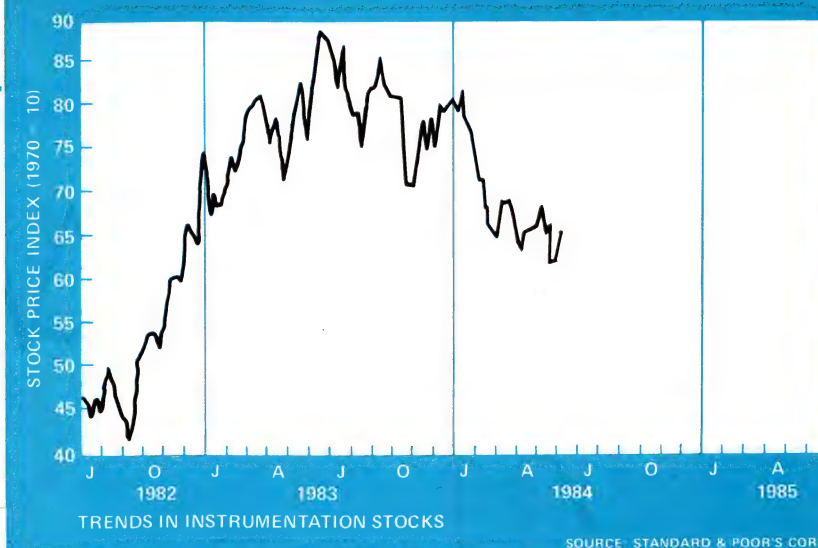
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## Business activity

### "Trends in instrumentation stocks"

records the stock market activity of a selected group of publicly owned manufacturers of test, measurement, and analytical instrumentation. The index weights the companies by size and therefore reflects their relative performances.



**Research and development expenditures** by the 100 biggest corporate spenders increased 9.9% in 1983 to a record \$32.1 billion, and spending this year could jump even higher. Those are the findings of the ninth annual survey of corporate R&D spending, conducted by Inside R&D, a publication of *Technical Insights Inc.*, Fort Lee, N. J. The survey notes that these companies' 1983 gain in spending was significantly smaller than the double-digit increases of recent years, although those increases were minimized by higher inflation. Still, last year's advance was greater than most forecasters anticipated. "The improvement in the economy that began in late 1982 is credited with the better-than-expected level of company-funded R&D spending," the survey says. "Projects remained in the pipeline that might have been canceled, delayed, or downgraded had the recession continued." As for 1984, preliminary indications are that company-sponsored R&D spending could rise 12.5%, the survey says.

Among the top 10 R&D spenders, IBM Corp. moved into second place, with 1983 spending of \$2.514 billion, up 22.5% from 1982 and behind General Motors Corp.'s \$2.602 billion. Predivestiture AT&T Co. slipped to third place, with 1983 spending of \$2.491 billion, up 19.7%. Elsewhere among the top 10, United Technologies Corp. was fifth, with 1983 spending of \$971 million, up 16.3%; General Electric Co. was seventh, with spending of \$919 million, up 17.7%; and Xerox Corp. was 10th, with R&D spending of \$555 million, down 1.8%. R&D expenditures as a percentage of sales averaged 5.06% for the top 100 firms in 1983, according to the survey, compared to 5% in 1982.

**Company financings**... Manufacturers of automated design tools for the electronics industry are scoring in the venture capital markets. A second round of financing brought \$3.7 million to *Cadtec Corp.*, a San Jose, Calif., maker of electronic-engineering design systems. Investors included *Tektronix Inc.*, Beaverton, Ore., which obtained a major equity position in Cadtec and signed a marketing agreement with the company... Work-station designer *Silicon Graphics Inc.*, Mountain View, Calif., completed a \$16.7 million second round of financing... Third-round venture financings raised \$12 million for *CAE Systems Inc.*, Sunnyvale, Calif., another maker of design tools, while *Cadnetix Corp.*, a Boulder, Colo., manufacturer of design-automation systems, received \$8.3 million.

—Robert J. Kozma



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## **Low-cost work stations shown at design show**

In an attempt to put a work station on every engineer's desk, three makers of computer-assisted-engineering gear are displaying stripped-down systems, supporting both logic-design and office software, at the Design Automation show in Albuquerque, N. M., this week. The prices of the new stations range up to \$30,000, compared to the \$50,000 to \$100,000 of current systems. Daisy Systems Corp., of Sunnyvale, Calif., has adapted its schematic-capture Logician software to the IBM PC XT, which it has beefed up with a new graphics controller and a high-resolution screen. **The Personal Logician is priced at \$17,000 and includes an Ethernet interface** so that it can share a data base with its upscale CAE cousins. Valid Logic Systems, of nearby Mountain View, has redesigned its Motorola 68010-based Scaldsystem hardware into a package that supports all Scald software, from logic capture to simulation, in a package that will sell for \$20,000 in a 16-station configuration. And Mentor Graphics Corp., of Portland, Ore., offers its Apollo Computer DS300 hardware in a network-compatible version that provides schematic capture and file sharing in a \$30,000 package.

## **IR offers cash for failed MOS FETs**

By offering a limited cash warranty on its MOS field-effect transistors, International Rectifier Corp. has come up with what veteran observers call a new wrinkle in marketing semiconductors. In effect, the El Segundo, Calif., firm is picking up the tab for any significant failure of its power MOS FETs if it occurs while they are in the hands of a customer. First available only to IR's ship-to-stock customers, whose devices go directly into inventory without inspection, it will be expanded to all buyers. **The goal is to cut down on incoming inspections, which the company says damage more devices than any other link in the delivery chain.** The basic condition is \$10 for each part failing in the field at a rate of more than 0.0019%/1,000 h at a junction temperature lower than 90°C. Competitors in the hotly contested power-MOS-FET field are withholding comment, but one has this unofficial opinion: "It could be an effective advertising gimmick, but only time will tell if it is more than that."

## **PlessCor, backed by Plessey-Corning, plans fiber-optic components**

A new company formed to fill what its principals say is "a product void for high-performance components for fiber-optic communications in the U. S." expects to be making them in a Los Angeles plant by early 1985. PlessCor Optronics Inc. has financial backing from major players in this fast-growing field: Corning Glass Works, a leading U. S. fiber producer, and Plessey Co. plc, the British firm that has pioneered the design and production of components. **PlessCor's founder is Michael K. Barnoski, a well-known research scientist in optics** who until 1983 headed such activities at TRW Inc. Serving as a board member and consultant is Theodore H. Maiman, who demonstrated the first laser while at Hughes Aircraft Co. and most recently worked at TRW. At first, the new firm will manufacture products developed by Plessey.

## **Data General unwraps its CAE family**

The latest in a rush of new products and marketing thrusts from Data General Corp. is its entry into the field of computer-aided-engineering and -design work stations. The Distributed Systems (DS) series combines the high-performance calculation capability of the Eclipse MV/4000



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## Digital hf radio breaches military solid analog wall

by Wesley R. Iversen, Chicago bureau

Rockwell-Collins unit for Canada made feasible by off-the-shelf availability of signal-processing parts

**Digital technology** is beginning to crop up in military radios, still largely the province of analog techniques. For example, Rockwell International Corp.'s Collins Defense Communications division, in Cedar Rapids, Iowa, is attacking that bastion with a new high-frequency radio receiver that employs digital signal processing of intermediate frequencies.

Designated the HF-2050, the single-sideband unit is said to be the first hf receiver to employ digital techniques in a production model. Under a \$6.5 million contract, Rockwell will deliver 1,016 of them over the next 15 months to the Canadian Department of National Defense. The U.S. military is also interested (see "U.S. Army pricks up ears at digital hf," p. 46).

The Canadians plan to use the receiver for domestic units and NATO forces in surface ships, submarines, and ground stations for communication with air and naval forces. Initial public showing of the radio came at the Armed Forces Communications and Electronics Association Conference & Exposition in Washington, D.C., last week.

Though the use of digital signal processing in radios has been on the drawing boards, the method is only now becoming cost-effective, one of the reasons being the off-the-shelf availability of special-purpose signal-processing microprocessors and other

very large-scale integrated circuits, explains Roger A. Kylo, Collins manager of hf-product engineering. In the 2050, only the portion of the receiver traditionally known as the intermediate-frequency strip has been digitized; conversion of the front-end receiver functions from analog to digital awaits the coming of even faster and more densely integrated components, Kylo observes.

**I-f tasks.** For competitive reasons, Collins officials will not describe specific components used in the 2050. But Kylo does note that either four or five signal-processing microprocessors are used, depending on options, to perform such classical i-f functions as conversion and filtering. These are performed on a digital signal supplied from an analog-to-digi-

tal converter sampling a 3-megahertz i-f signal at 12 million samples per second. After digital processing, a digital-to-analog converter transforms the signal at a 16,000-sample/s rate for audio output.

The advantages of digitizing the 2050's i-f strip include improved reliability and manufacturability, thanks to a lower parts count and a higher percentage of automatically insertable components. The unit uses only 2,000 components, compared with about 3,500 needed in a comparable all-analog receiver—a reduction of more than 40%—while board area and cabinet dimensions are decreased by about 30%. Mean time between failures will be specified at about 5,000 hours for the 2050, compared with a typical 1,000 to 2,500 h on



**By the numbers.** Rockwell's Collins operation uses digital signal processing for hf in this general-coverage receiver that also operates with very low, low, and medium frequencies.



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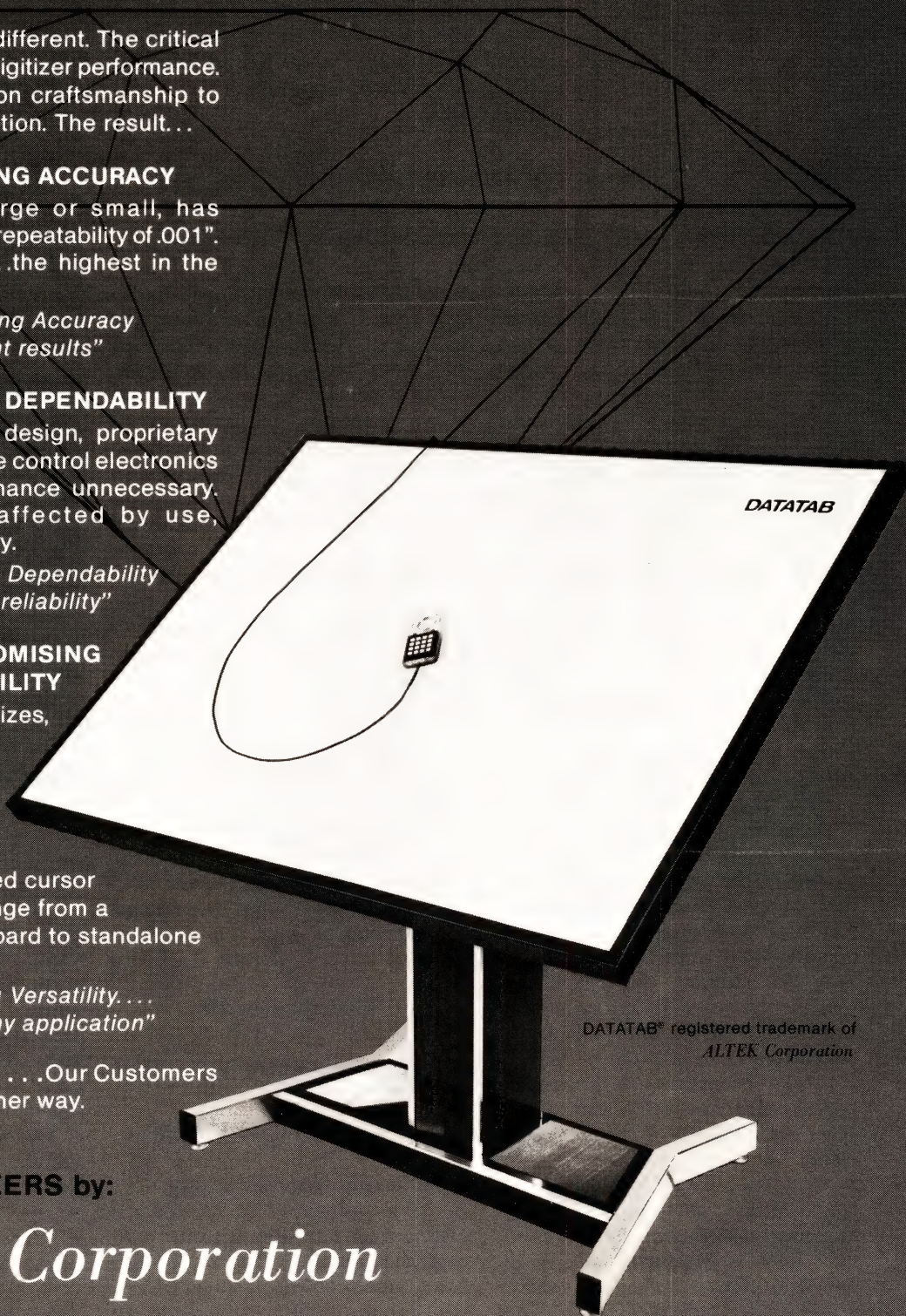
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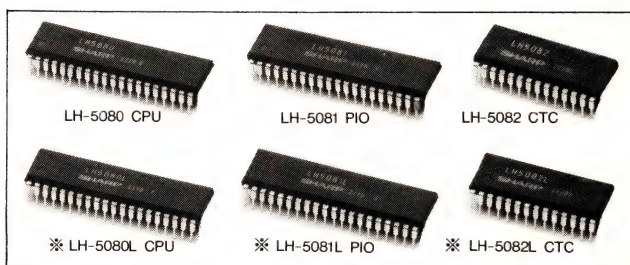
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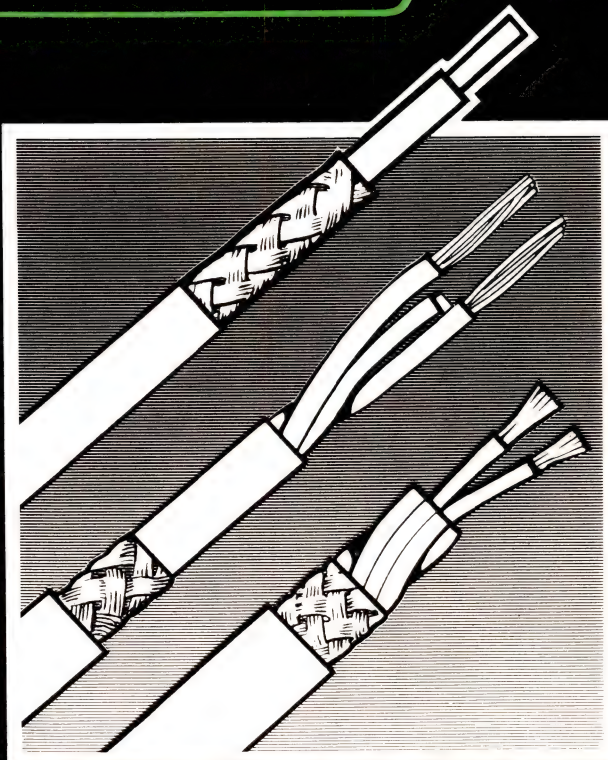
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states. "IBM has never had to understand the PC standard to the degree that Compaq has because it means survival to us."

The 8086 and 8088 microprocessors are made by Intel Corp., Santa Clara, Calif., and both chips have internal 16-bit architectures. However, the 8088 has an 8-bit data bus, and the 8086 a 16-bit data bus.

**Two times faster.** The new DeskPro has a 7.14-megahertz 8086 central processor and is capable of running PC-DOS software two to three times faster than a 4.77-MHz 8088-based system, says Gary Stimac, director of engineering for Compaq's recently created Office Computer division.

To do this, Compaq system designers divided the DeskPro architecture into two bus structures, which are married through a series of state and bus controllers implemented in programmable logic arrays. The system bus, which accepts peripheral and expansion boards designed for the PC, is 8 bits wide. Data traveling on the byte-wide bus is converted to a 16-bit bus for the 8086 and main memory.

One of the engineering challenges was getting the 8086 to act like an 8088, Stimac says. A system with Compaq's version of the PC-DOS 2.11 operating system will automatically shift from one speed to another depending upon the application software. The system can also run older versions of PC-DOS, but in those cases, speed modes must be changed from the keyboard.

Compaq's DeskPro will be available in four models. That includes one at the top end that sells for \$7,195 for 640-K of random-access memory, a single half-height 5¼-inch floppy-disk drive, 10 megabytes on a fixed 5¼-in. Winchester disk, and 10 megabytes of cassette-tape backup storage.

At the low end, the DeskPro Model 1, with 128-K of RAM and a single 5¼-in. floppy-disk drive, will carry a price tag of \$2,495. The firm says a single DeskPro cabinet can hold two floppy-disk drives and one Winchester drive along with a cassette-tape backup drive. —J. Robert Lineback

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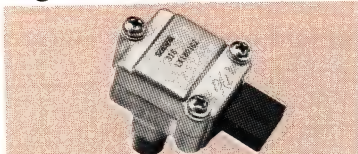
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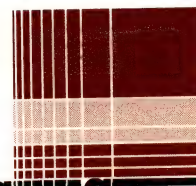
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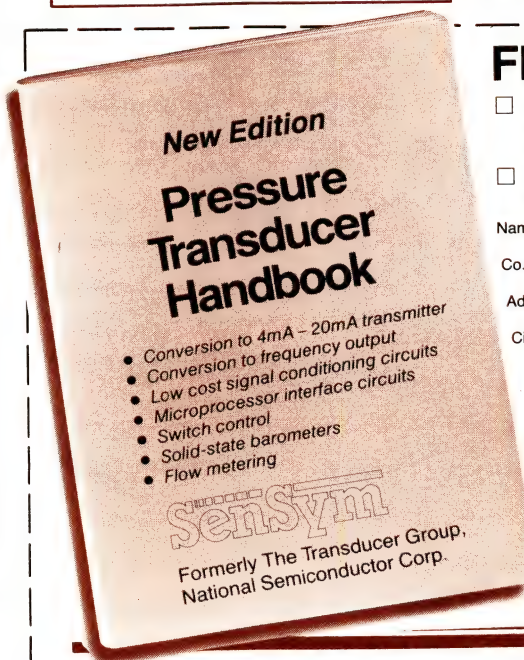
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## **Congress toughens Federal purchasing**

Competition for the Government's business is going to get a lot tougher now that House and Senate conferees have agreed on a bill reforming Uncle Sam's procurement system. The key legislation is the competition-in-contracting act, which will severely reduce the circumstances under which Federal agencies, including the Pentagon, can bypass competitive bidding through the issuing of sole-source contracts. In the past, sole-sourcing could be justified by "practicability"; now it must be an emergency, or high-level national security and procurement officers must sign off on the contract stating so. **Over the next three years, the bill's effect on competition should mean at least a \$6 billion savings to the Government,** as well as new opportunities for small businesses, says the Congressional Budget Office.

## **NASA outlines plan commercializing space**

Hearings held by the House in late June offered a preview of the National Aeronautics and Space Administration's long-awaited study on what Washington should do to promote commercial ventures in space. Industry witnesses who helped draft the report's final recommendations highlighted a number of economic incentives. Among them are the extension of research and development tax-credit allowances to space-based businesses; mechanisms such as Government-guaranteed loans and bonds to attract space venture capital; measures to facilitate insurance coverage for spacecraft owners; and rate reductions for shuttle flights. To further offset initial investment risks, **NASA is planning to make its research facilities and personnel available to industry** for projects with a reasonable chance of leading to commercial products, said the agency's administrator, James M. Beggs.

## **Adapso scores plan for Federal sponsorship of educational software**

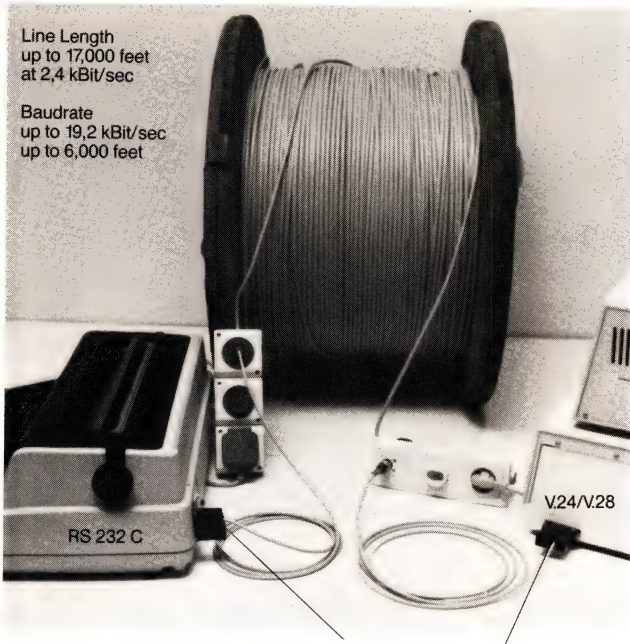
At least one computer industry association fears Federal influence over the choice of educational software used in the nation's elementary and secondary schools if the Computer Literacy Act becomes law. The measure has just been reported to the House by the subcommittee on Science, Research, and Technology. Sponsored by Rep. Timothy E. Wirth (D., Col.), the bill would grant \$20 million for teacher training by a non-profit organization and \$14 million to the National Science Foundation and the National Institute of Education to develop model educational software. The latter, charges the Association of Data Processing Service Organizations, **could result in a de facto Government standard "at the lowest possible level."** In addition, the act sets an unspecified amount aside for schools to buy some 1.3 million microcomputers—another provision Adapso faults because it does not include the purchase of software. The hardware procurement could cost the Government more than \$2.2 billion, estimates the Congressional Budget Office.

## **Senate okays R&D funding for universities ...**

More to industry's liking is the Senate's Manufacturing Sciences and Technology Research and Development Act, cleared by the full body in mid-June. Seen as a positive alternative to the more comprehensive industrial-policy legislation awaiting action in the House, the bill calls for the Department of Commerce to disburse some \$45 million to universities starting in 1985. To receive any money, the institution would have to get a company or consortium to match the amount. Rather than



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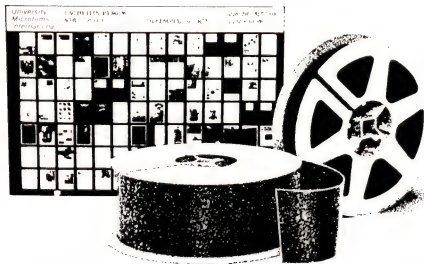


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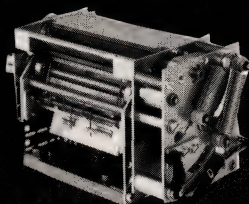
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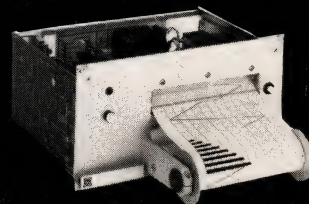
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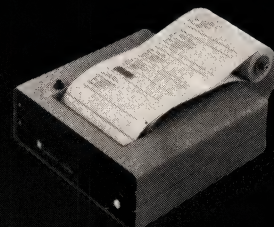


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# International newsletter

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## **MITI plans assistance to high-tech firms ...**

Japan's Ministry of International Trade and Industry is drafting legislation that would provide tax and financial assistance to firms active in such leading-edge technologies as ceramics, microelectronics, and biotechnology. **MITI says the move is designed to close the research-outlay gap between the U. S. and Japan.** In 1982, research in nondefense projects sponsored by the U. S. government cost \$39 billion, compared with just \$7.4 billion for Japan, MITI claims. The ministry estimates that the world information-processing and electronics market will be worth \$104 billion annually by 1990, while world markets for new materials and biotechnology will grow to about \$43 billion and \$31 billion, respectively, by the year 2000.

## **... while AEA Tokyo office seeks to ease U. S. entry into Japanese market**

Now open for business is the office that the American Electronics Association has set up in Tokyo to promote its interests in that country and to serve as a watchdog for U. S. electronics firms. **The office has several immediate priorities: monitoring the efforts of the Ministry of International Trade and Industry to regenerate a controversial software-protection law and giving U. S. engineers access to Japanese government research and development projects,** as well as generating a Japanese electronics newsletter for AEA members. John P. Stern (see p. 14), a Japanese-speaking lawyer with a background in trade issues, is the senior representative in the AEA-Japan office, which includes another full-time staff member and two temporary researchers. The office has been set up with a two-year seed-money grant of \$250,000 annually from the U. S. Department of Commerce.

## **German electronics expects a good year despite strikes**

In the face of strikes by metal workers in much of West Germany, electrical and electronics executives are optimistic that their industries can sustain growth of better than 4%—about twice the 1983 level—for the rest of this year. **Strikes and lockouts by mid-June had idled more than 300,000 people in the metal-working, automobile, and electronics industries.** They concern demands for a cut of the 40-hour week with no cut in pay. Of course, without these troubles, the overall growth of the electrical and electronics sectors would have been higher, but industry officials think that demand for high-growth items will offset such no-growth areas as electrical machinery and power plants, which are included in the figures. The market for electronic components will enjoy one of this year's highest gains over 1983 levels. In 1984, sales of ICs alone are predicted to rise by nearly 50% and those of discrete devices by more than 20%. During the first third of this year, sales of data-processing and communications equipment were 33% and 17% higher, respectively, than they had been during the same period in 1983.

## **Europeans love IBM's PC**

Although the number of personal computers currently in use for business applications proportionally lags well behind U. S. levels, Europe's installed base of IBM Corp. Personal Computers will grow by at least 200% this year, enough to dwarf penetration by all of the U. S. company's competitors. According to a multiclient study by Intelligent Electronics Europe, a Paris-based market research firm that interviewed more than 300 European companies, **the reason most buyers chose the IBM PC was quality of service and availability of software.** Price was



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# Instruments and Collins Avionics dense circuit reliability soar.

board caused the solder joints attaching the components to the board to break.

TI's solution: A composite metal core of low-TCE Invar that is clad on both sides with copper. Thin, polyimide-glass, multilayer boards were bonded to each side of the metal, to provide the circuitry function.

With a TCE match between the board and the chip carriers, the PC boards easily passed the exacting thermal cycling tests.

And the metal core in the board dramatically improved thermal conductivity and overall rigidity.

## Solves thermal mismatch problems

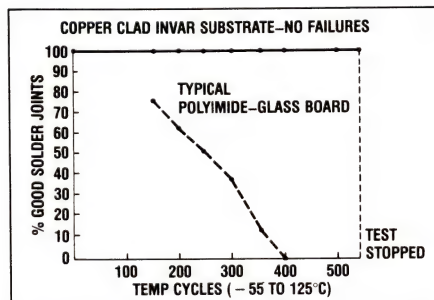
As Collins Avionics discovered, the advantage of using chip carriers to achieve high-density, high-performance circuitry also imposes stringent demands for increased thermal management, structural integrity, as well as TCE compatibility—demands met by Texas Instruments copper-clad Invar.

By combining TCE compatibility with high lateral thermal conductivity. And mechanical rigidity.

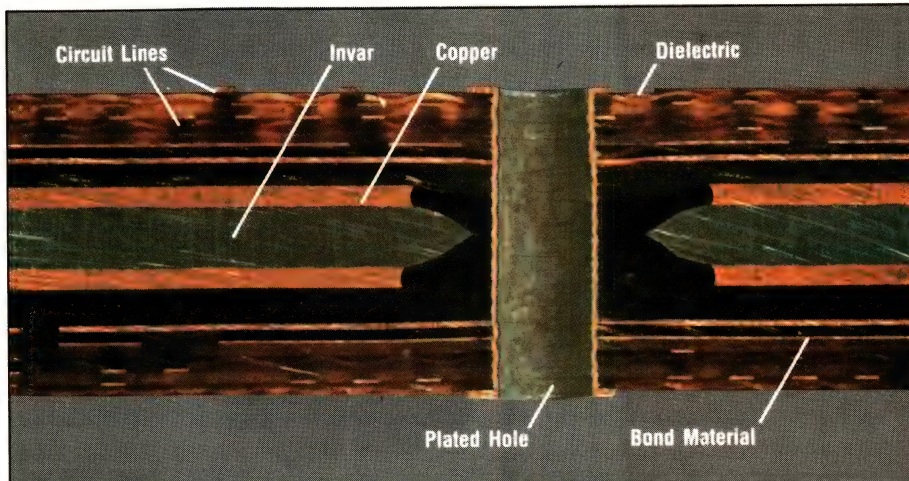
All at lower cost than alternate approaches. ■

## The solution is a trilayer metal.

TI's process involves roll bonding copper foil to Invar—a 36% nickel/64% iron



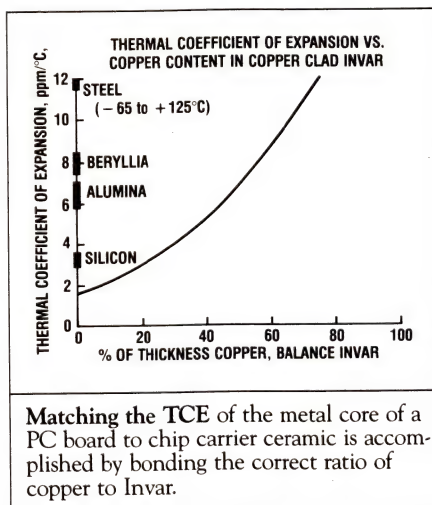
After 540 thermal cycles from -55° to 125°C failed to break chip carrier solder joints, Collins Avionics halted tests of PC board used in F-15 communications system. Reliability goals had been surpassed by a wide margin.



Effective thermal management is achieved with a copper-clad Invar core that acts as a support for circuitry in the PC board. Heat dissipation characteristics of the copper are excellent, and the Invar contributes rigidity and strength.

alloy. The bonding to each side of the Invar is accomplished by the same process used to make thermostat metal and coins. No adhesives or brazing alloys are required to achieve a permanent bond.

By varying the ratios of the high thermal conductivity copper to the ultra-low TCE Invar, the TCE of the clad metal can be tailored to match that of silicon, alumina, or beryllia.



Matching the TCE of the metal core of a PC board to chip carrier ceramic is accomplished by bonding the correct ratio of copper to Invar.

This material is available in thicknesses from 5 to 62 mils (.13 to 1.57 mm). You can get it in widths up to 24 inches (610 mm).

Copper-clad Invar is being developed for many other applications: From ground and power planes in multilayer boards,

to heat sinks and covers for multichip ceramic modules, and more.

## A clad remedy to packaging challenges

TI's innovative clad metal solutions can solve your circuitry packaging problems—with a variety of materials.

You can get copper-cored electron tube materials; nickel-clad stainless steel transistor can materials; copper-clad stainless steel lead frame materials; precious metal, aluminum, and solder selective cladding on base metals for lead frame and connector applications; copper-clad steel, aluminum, and Alloy 42 wire products; and high-speed precision stamping and assembly.

In fact, TI—the world's leading clad metals manufacturer—can help you develop a clad metal solution to many electronic materials problems.

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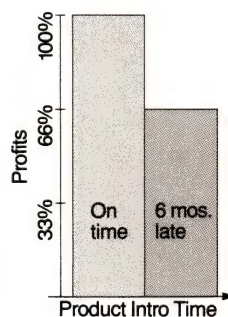
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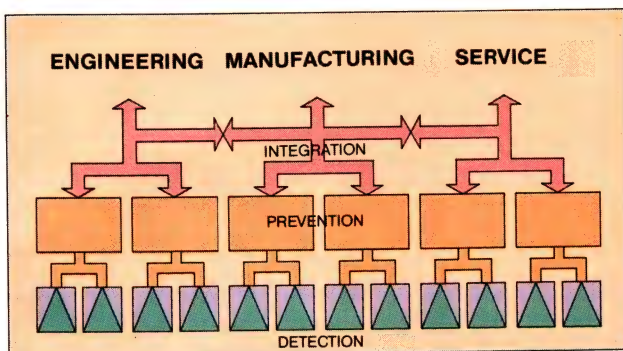
When you manage quality, you can improve the *process* that creates your products.

You can *prevent* faults instead of just finding them.

But first, you must learn how to leverage your ATE investment.

### How to leverage your ATE investment.

Any systematic approach to Quality Management must start with the data created by ATE.



There are three levels of Quality Management. Level 1 is fault detection. Level 2 is fault prevention. Level 3 is the integration of quality information throughout the entire process. As you can see, Quality Management builds up from a solid base of testing capability.

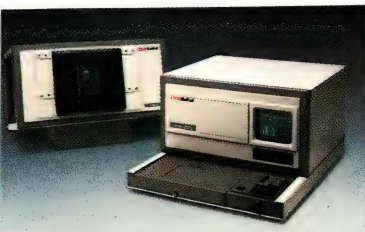
There's simply no place else to get it. But that data by itself won't help you improve quality. Unless you *leverage* it.

To leverage, you must apply powerful Quality Management Software to sort reams and reams of test data. And extract meaningful quality information.

Then you must put that quality information to use where it can do you the most good.

When you leverage, you'll be able to identify trends. You'll be alerted to emergency situations. And you'll be able to monitor the extent of improvements in quality. Automatically and in real-time.

As a result, you'll be able to actually manage and improve quality. And you'll get a better return on your ATE investment.



### The solution is at hand today.

Quality Management is not some futuristic notion.

But to make Quality Management work, you do need three things.

First, you need ATE. And GenRad offers the broadest line of ATE in the industry.

Secondly, you need to learn to leverage. Again, GenRad offers the tools you need, hardware and software, that can help you move to higher levels of quality.

Already, several of our Quality

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And SCAN™ – a system that helps you improve the quality of incoming compo-

nents and the productivity of your incoming inspection process.

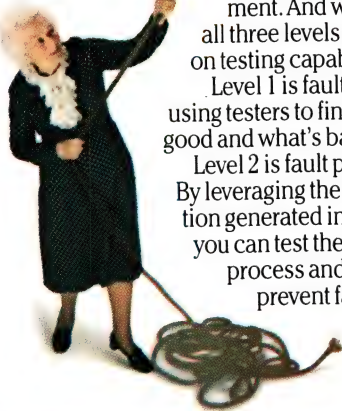
Finally, you need a company that's willing to work with you in solving your special problems. GenRad provides more of that kind of custom applications support than anyone in the industry.

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At GenRad, we believe there are three levels of Quality Management. And we believe all three levels depend on testing capability.

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When you use leverage, you can perform tasks that would be otherwise impossible. GenRad can show you how leveraging your ATE investment can dramatically improve quality.

of just finding them.

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AUTOMATING QUALITY MANAGEMENT



## Phase shift plots chromatic dispersion in monomode fibers

by Robert T. Gallagher, Paris bureau manager

Two light-emitting diodes work  
in consort with other kinds  
of simple and conventional  
optical and electronic hardware

A solution may now be at hand to one of the major stumbling blocks holding up the industrialization of high-performance optical-fiber networks: precise, easy, and inexpensive measurement of chromatic dispersion in monomode optical fibers.

Accurate measurement of chromatic dispersion is essential to optimize optical communications, both for transmission capacity and the spacing of repeaters in an optical link. While a number of experimental measurement techniques have been so used with success, there is a snag: until now, they have all required unwieldy configurations that are out of the question for industrial or field environments as well as being prohibitively expensive.

A way around this apparent impasse has been found by researchers working at the Centro Studi e Laboratori Telecomunicazioni (CSELT), in Turin, Italy, who have developed a system based on a phase-shift technique that measures chromatic dispersion in monomode fibers using two reliable and low-cost light-emitting diodes in consort with other kinds of simple and conventional optical and electronic hardware.

By such standards as accuracy, wavelength resolution, and ease of operation, the net result is an attractive and practical alternative to better-known schemes based, respectively, on neodymium yttrium aluminum

garnet lasers and the Raman effect, changes in the frequency and random alternation of phase as light passes through a transparent medium. In addition to the two LED sources, the CSELT measuring setup consists of a signal generator, a monochromator, a vector voltmeter, and a detection module—all controlled by a microcomputer.

On the transmitting side, LEDs of indium gallium arsenide and phosphorus are coupled to the fiber to be tested through a standard 50/125 multimode pigtail. A monochromator selects different wavelengths within the LED spectrum. A quartz oscillator generates the signal and modulates the LEDs at 30 megahertz.

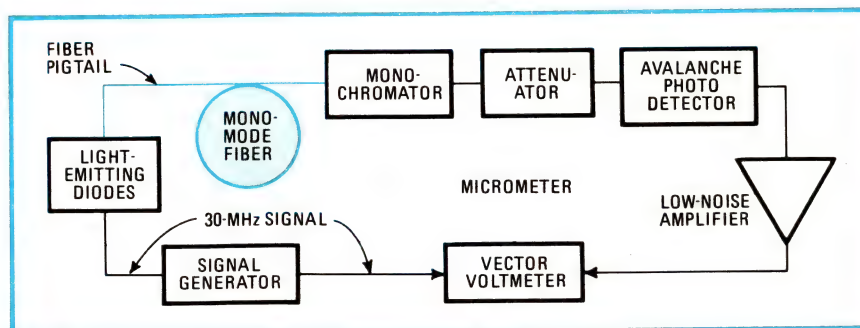
On the receiving side, a germanium avalanche photodetector and a low-noise amplifier detect the optical signal. The phase of the 30-MHz optical signal is read by the vector voltmeter, which compares it with the 30-MHz electrical signal supplied by the quartz oscillator. To allow for wavelength phase shifts resulting from anything besides the fiber—chromatic delay by the LED is the most common example—a calibration

measurement is carried out on a short (about 1-meter) length of fiber. The optical signal used for testing is fixed at the level that an optical attenuator obtains during calibration.

The two LEDs have center wavelengths of 1.33 and 1.47 micrometer, respectively, so they can cover transmission wavelengths from 1.2 to 1.6  $\mu\text{m}$ . Other devices can extend spectral coverage downward to 0.75  $\mu\text{m}$ . The sources are operated at constant temperature to avoid phase drifts caused by thermal factors.

**Two ways.** Computation of a fiber's chromatic-dispersion curve takes place in two steps. First, chromatic delay in nanoseconds per kilometer of fiber is plotted against corresponding wavelengths. When these experimental points have been connected to form a suitable equation, that curve is differentiated to produce a curve of chromatic dispersion versus wavelength.

To verify the method's accuracy, CSELT engineers conducted chromatic-dispersion tests on a 1,360-meter length of Corning Glass fiber with a 0.5-decibel-per-kilometer attenuation at a 1.3- $\mu\text{m}$  wavelength. They com-



**Simpler and cheaper.** Using this configuration based on LEDs and standard electronic and optical components, the Centro Studi e Laboratori Telecomunicazioni has devised a low-cost, highly accurate method of measuring chromatic dispersion in optical fibers.



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| 2N6792           | IRFF320         | 1.8                      | /555                     | TO-39      |
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| 2N6796           | IRFF130         | 0.18                     | /557                     | TO-39      |
| 2N6798           | IRFF230         | 0.4                      | /557                     | TO-39      |
| 2N6800           | IRFF330         | 1.0                      | /557                     | TO-39      |
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| 2N6758           | IRF230          | 0.4                      | /542A                    | TO-3       |
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| 2N6762           | IRF430          | 1.5                      | /542A                    | TO-3       |
| 2N6764           | IRF150          | 0.055                    | /543A                    | TO-3       |
| 2N6766           | IRF250          | 0.085                    | /543A                    | TO-3       |
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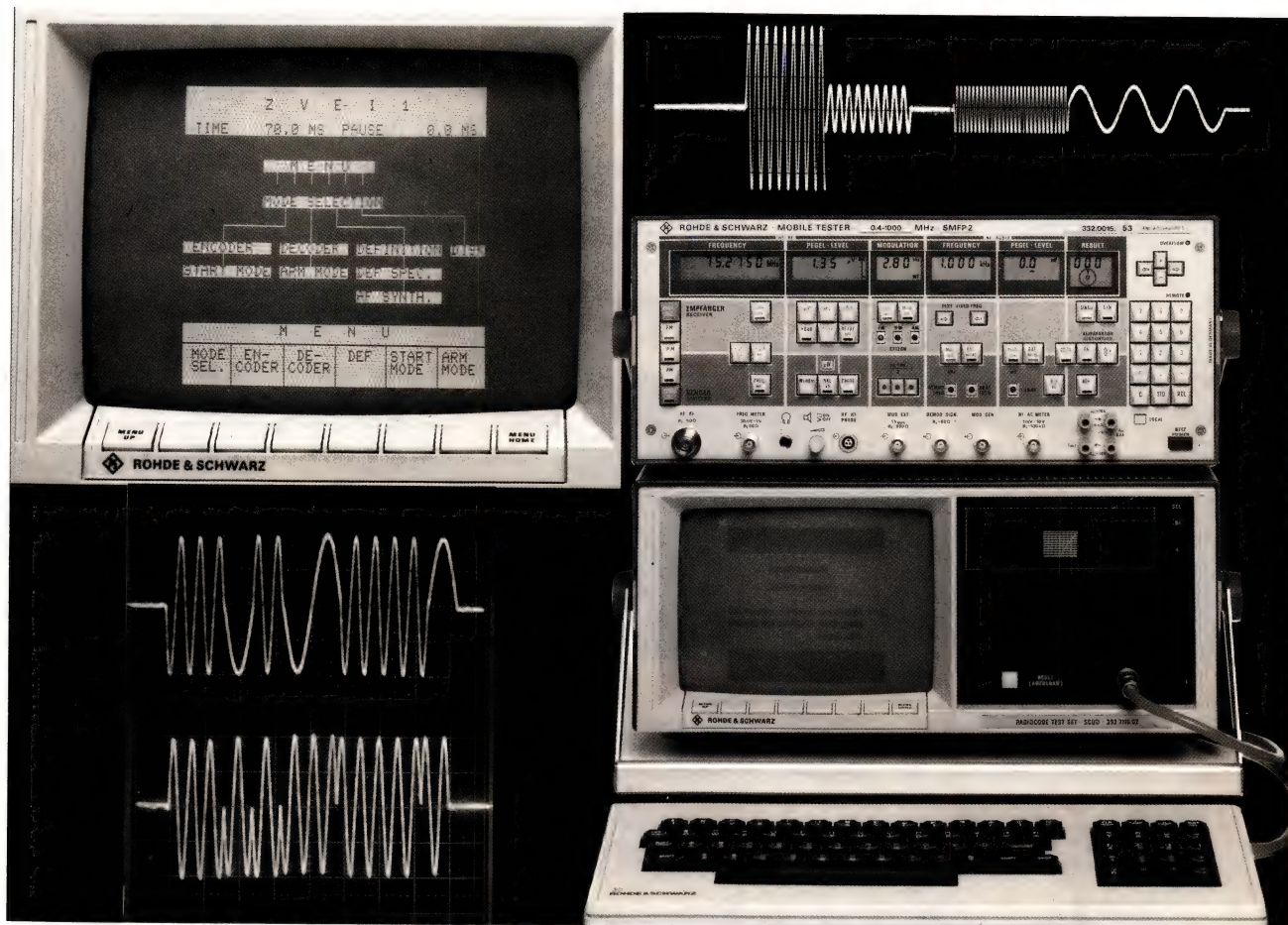




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## Stern plays difficult role as U. S. business ambassador

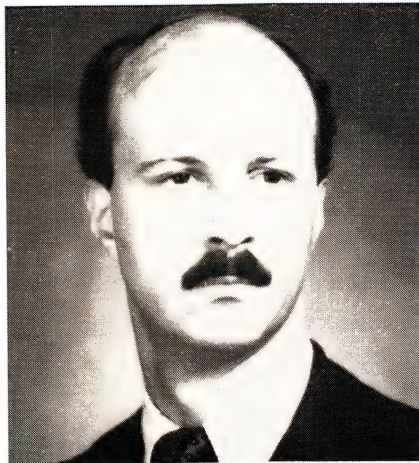
When John P. Stern studied Japanese history at Princeton University, his senior thesis dealt with Japan's acceptance of Western legal and political ideas during the Meiji Restoration. The recently appointed senior representative of the American Electronic Association's Tokyo office, which opened June 1, is now going to see if the Japanese will give fuller acceptance to another Western idea: equal market access.

"We didn't establish this office to engage in Japan-bashing," says Stern, "but we want to educate more Japanese to the need to liberalize their markets further and to educate our own membership about the market opportunities which exist here."

Stern, who earned a law degree from Harvard University, comes to the AEA after nearly six years with Graham & James, a San Francisco-based law firm, where he helped Japanese software houses do business in the U. S. Now he is working in the opposite direction because one of the first projects will be to monitor the efforts of Japan's Ministry of International Trade and Industry to revise a software-protection law and reintroduce it to the Japanese Diet this fall [*Electronics*, May 17, p. 24].

The AEA-Japan office, set up with \$250,000 in seed money from the U. S. Department of Commerce to assist the first two years of operation, will also try to help U. S. electronics firms get access to Japanese research and development projects. The objective is to involve U. S. engineers in the setting of specifications for electronic products and systems in the Japanese market.

As a start, the AEA has set up a pilot program that will send six U. S. graduate students in electrical engineering or computer sciences to a summer Japanese-language course. Starting this September, a number of firms—including NEC Corp., Intel-Japan Corp., and Oki Electric Industry Co.—will pay all the students' expenses for up to nine months of work in corporate research laborato-



**AEA voice.** As the American Electronic Association's Tokyo representative, John P. Stern will try to get equal market access.

ries and institutes.

Apart from representing the AEA, Stern says that he and his staff of three will also serve the interests of the Semiconductor Industry Association, since 95% of its members also belong to the AEA. He adds that in the future there might be an AEA-SIA office in Tokyo.

## Realizing all our fantasies, they buy out the boss

Alan Mansfield and Tony Jannece are members of a small but growing elite: executives who purchased their business from their former employers. In April, the two acquired Gould Advance Ltd.'s power-supply manufacturing operation from the Hainault, Essex, company. The new

company, located in Bishop's Stortford, Essex, is now trading as Advance Power Supplies Ltd.

Such management buyouts, though common in the U. S., are a comparatively recent phenomenon in the UK, pointing to an increasing entrepreneurial vigor in the business environment. Both Jannece, 53, chairman of the new company, and Mansfield, 45, the managing director, worked for Advance Electronics Ltd. prior to its 1974 acquisition by Gould.

Jannece was then the financial director, and he went on to hold several senior management positions with Gould, most recently as chairman of Gould Instruments Ltd. Mansfield returned to the UK in May, 1983, after three years as president and general manager of Gould Inc.'s Instrument division in Cleveland, Ohio.

The chance to buy what was Gould's Dc Power Supply operation came when the U.S. firm announced in October, 1983, that it intended to sell its Power Conversion division—which included the ac power conversion plant in San Diego, Calif., that the English team did not take over—because it did not fit with Gould's strategic objectives. Mansfield and Jannece, backed by a group of investors, successfully bid for the operation in the face of stiff competition from companies in the UK and U. S.

The two partners have purchased one of the top European manufacturers of dc power supplies, with sales of \$14 million per annum and sales offices in Germany and the U. S. The company's Bishop's Stortford plant has been equipped with the latest automated production and test equipment, including computer-controlled scheduling.

Jannece and Mansfield, who hold a controlling interest in the company, intend to develop and expand the existing product range with several new products in 1984. Initially, there will be a greater emphasis on European sales, as U. S. outlets received a great deal of attention under Gould.



**New bosses.** Alan Mansfield (left) and Tony Jannece (right) purchased Gould's Power Conversion division and are revitalizing and expanding its product offerings, placing greater emphasis on sales in Europe.



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# Military system used for education bows in civvies

by Robert Gallagher, Paris bureau

Portable CAE system is based on iAPX 432, has the power needed for real-time simulation and interactive graphics

Nearly three years ago, when Matra S. A. went shopping for a computer-aided education system to sell along with military systems requiring rigorous training programs, the Parisian company found that nothing on the market filled its need for a relatively portable though powerful system—so it developed its own. Now, with the system up and running, the company is gearing up to take double advantage of the extensive hardware and software development the effort required by selling the CAE system as a product in its own right.

Matra found that available systems fell into two varieties—based either on microcomputers or mainframes—and both had basic limitations. Microcomputer-based CAE systems were portable and inexpensive enough but lacked the computing muscle needed for real-time simulation programs and interactive graphics. Mainframes remedied these limitations but were unacceptably expensive and, of course, completely unportable.

Matra's answer was to look for a dedicated processing configuration based on the most powerful available components. Engineers in the company's Military Systems division settled on the Intel iAPX 432 32-bit microprocessor, principally because it can be programmed in Ada, a language designed to connect diverse systems that function in real time—as in office-automation, industrial, and tele-

communications systems.

The result offers both the principal advantages of the two standard approaches: portability, on the one hand, and computational power for real-time simulation and interactive graphics, on the other. What's more, the unit is a multiperipheral and multimedia system that simultaneously uses a video screen, sound, and a graphics screen and can even employ real-time equipment, such as control panels.

Its modular nature makes it easy to integrate into existing or new CAE systems. Although originally developed for military training, the system's software is easily adaptable to any content. It takes the form of an expert system.

Physically, the system comprises two basic modules: the student post and the teacher post, each about the size of a standard office desk. The student post consists of a central unit housing the iAPX 432, a floppy-disk

drive, either a video tape recorder or a video disk unit, and a cassette tape recorder. The work surface has a command keyboard and screen, a video screen, and a graphics screen.

When students arrive for their courses, which can be either individual or group, they need floppy disks with the programs for their lessons, the related video-tape cassette or disk, and their personal cassettes. The personal cassette is what lets students access the system, and it also carries their course histories and thus permits teachers to follow their progress. A teacher can access all performance information on a student's cassette. The system can be programmed so that students are not given access to some, or even all, of this information.

The teacher's post is similar to the student's but has complementary tools to permit data entry. Courses can be designed in, either from scratch or by modifying existing pro-





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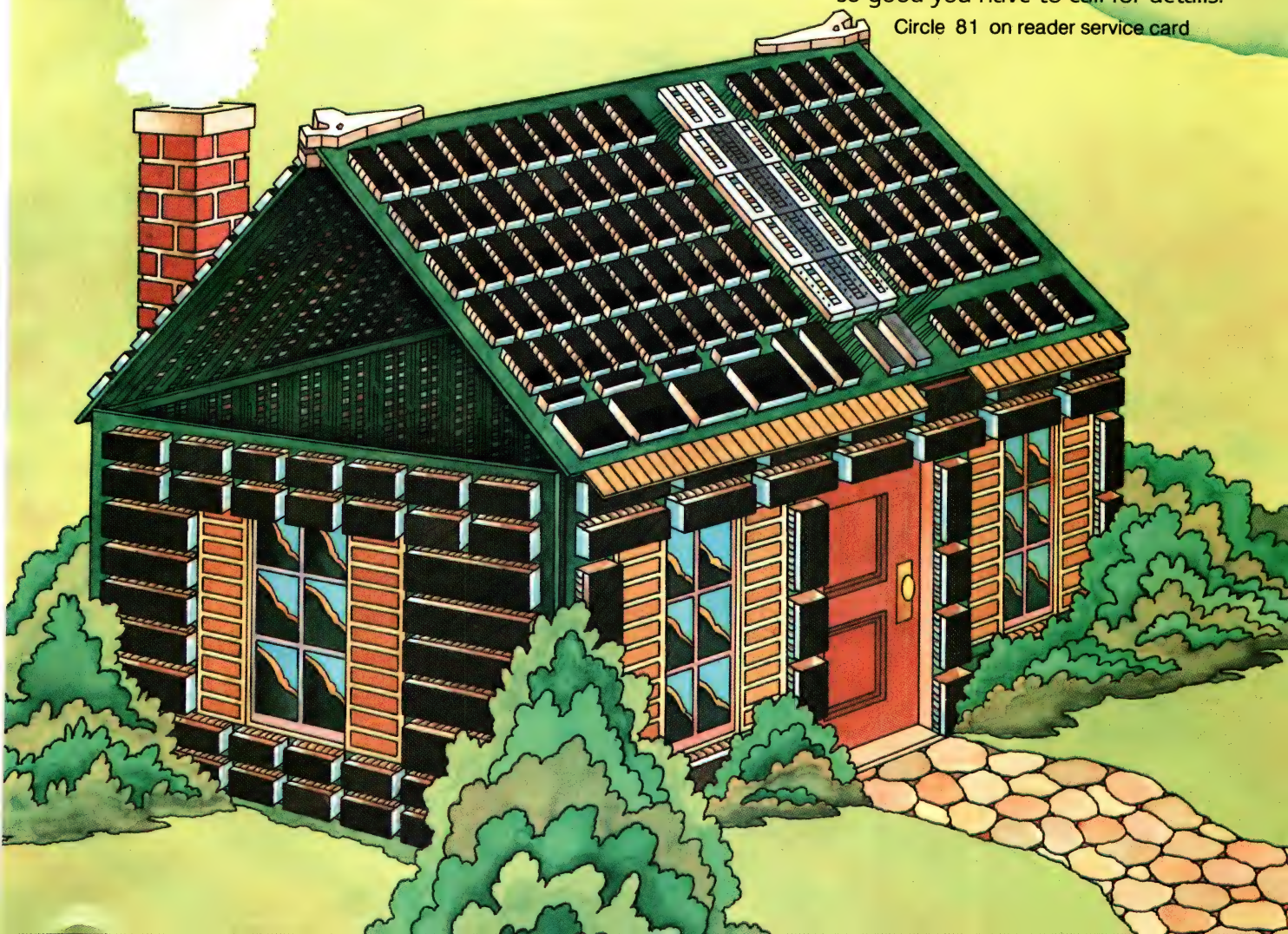
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# IS ENGINEERING



## Boom squeezes captive chip makers

Increased demand for semiconductor parts manufactured in house strains resources, slows firms' plans to enter the merchant market

by Wesley R. Iversen, Chicago bureau manager

**Captive semiconductor** manufacturers—those that build chips and other devices for internal company use—enjoy some degree of insulation from the rigors of the outside market. But as they seek to make more efficient use of their capacity and even out their businesses' cyclic nature, captive makers are increasingly moving to sell chips on the open market.

However, while it is a seller's market, the largest captives, like the major merchant vendors [*Electronics*, May 3, p. 47], cannot take on all the new business available because they are pushing to keep up with the current exploding demand for advanced semiconductor parts—in their case, in-house demand (see figure).

At AT&T Technologies, for example, plans to enter the merchant market have been hampered by internal chip demands while the firm scrambles to ramp up production capacity. Despite parent AT&T Co.'s status as the first U. S. company to provide samples of 256-K random-access memories more than a year ago, the firm now says there will be nothing of substance for new outside customers until at least the first quarter of next year (though small production commitments made to a few outside customers will be honored).

In the meantime, construction resumed last December (following an

18-month halt) on a 700,000-square-foot chip plant in Orlando, Fla. Expansion likewise is underway at existing plants in Kansas City, Mo., and Allentown, Pa., to add 256-K chip capacity.

IBM Corp. is also pouring plenty of cash into plant construction and advanced chip-processing, -packaging, and -testing gear. Already the world's largest manufacturer of integrated circuits, IBM is currently adding a combined total of 2 million ft<sup>2</sup> to its two major domestic fabrication plants in Burlington, Vt., and East

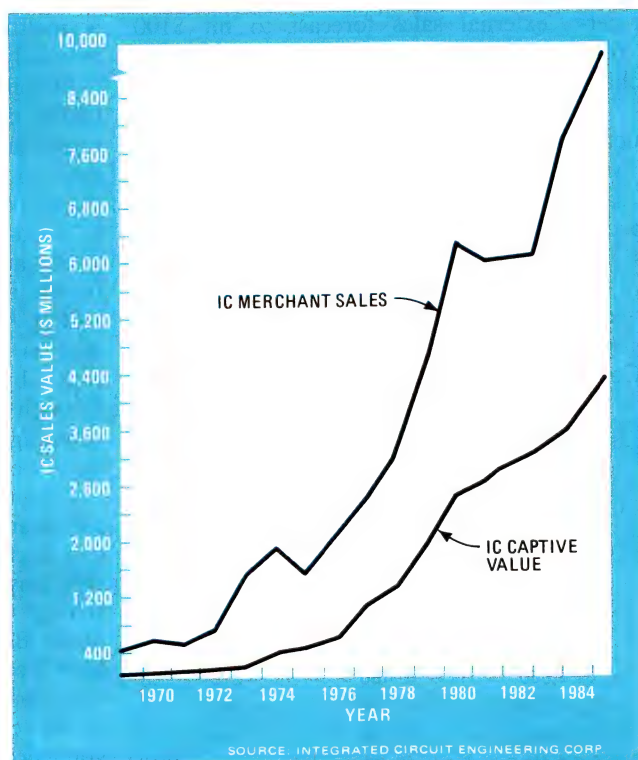
Fishkill, N. Y. Unlike AT&T Technologies, however, IBM seems to be aiming at insatiable internal needs, with probably no merchant market chips in the offing.

As the third largest captive-IC house (see table), General Motors Corp.'s Delco Electronics division is also feeling the heat. Compared with the 1981-82 recession doldrums, when Delco's Kokomo, Ind., unit was running at about 80% capacity, "We're now running at about 125% capacity utilization," declares Walter R. McIndoo, director of the semiconductor business unit. "We're running six and seven days a week."

Relief is on the way in the form of a \$60 million bipolar 5-inch-wafer fabrication line. Scheduled for first production in about a year, the line will turn out about 1,000 wafers per day, increasing Delco's total capacity by more than 30%, McIndoo says.

**Spreading out.** In spite of the current boom, Delco is in line with a growing captive industry trend by looking to expand sales to the outside market. "Eventually, we want as much as 40% of our business to be to non-GM customers," says McIndoo, who sees the percentage split about evenly between automotive and non-automotive sales. More than 90% of the semiconductor business unit's business now comes from the parent GM.

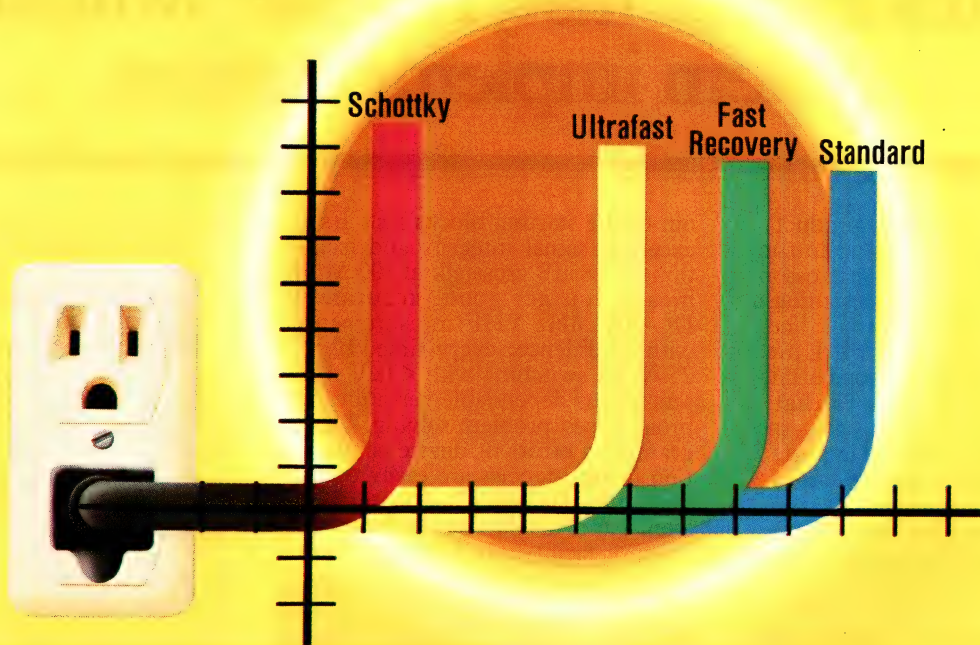
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**Growing.** Like chip suppliers in the merchant market, captive manufacturers of semiconductors are experiencing rising demand for their semiconductor components. This reflects the growing demand for products made by the captives' parent companies.



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| 30A TO-3            | •        |            |      |          |
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Information processing

## Array processors go upscale

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New "bargain-priced" 64-bit machines can take on some supercomputer jobs but they won't make multimillion-dollar Crays and Cybers obsolete

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by Clifford Barney, Palo Alto bureau

**Array processors**—those fast number crunchers used to offload repetitive computational work from mainframes and minicomputers—now have grown up enough to go out on their own. With the addition of megawords of high-speed memory and architectures that support 64-bit floating-point operations, they are achieving performance approaching that of supercomputers costing many times as much and finding applications as general-purpose scientific machines.

A Cray-1 supercomputer from Cray Research Inc. will run at 160 million floating-point operations per second and costs between \$5 million and \$10 million. By contrast, the FPS-164 processor, offered by Floating Point Systems Inc., provides 11 to 15 megaflops for \$300,000; and the Beaverton, Ore., firm recently announced an accelerator that will carry performance of the 164/MAX to an awesome 331 megaflops, in certain well-defined applications, for under \$1 million [*Electronics*, May 17, p. 162]. Another array-processor maker, CSP Inc., of Billerica, Mass., offers 5 megaflops for \$100,000, on its MAP 6420 equipment.

Floating Point Systems and CSPI are just the first entries in the 64-bit array-processor market, the bargain basement for supercomputers. Other firms undoubtedly will follow their lead. Most array-processor manufacturers put the present market for 32-bit machines—which currently

dominate the business—at \$200 million to \$300 million yearly, growing at about 20% to 25% a year.

The scientific and engineering market, largely the domain of the 64-bit machines, is much bigger. Floating Point's marketing vice president, John Harte, pegs it at \$2.7 billion. He figures it is growing at 25% a year, fueled partly by exotic new applications such as computer-aided design of everything from integrated circuits to drugs.

"In five years, anyone who is just an array-processor manufacturer won't be in business," says Bruce R. Mackie, sales and marketing director of Analogic Corp., Wakefield, Mass., one of the earliest array-processor manufacturers. "The 64-bit market is the future. Don't count Analogic, Star, or Numerix out of it." And Charles P. Burrows, marketing director of Quantitative Technology Corp., a Portland, Ore., supplier of application software to array-processor companies, says that in addition

to the established array-processor makers, several start-ups are ready to enter the 64-bit market.

**Dominant.** Meanwhile, 32-bit machines dominate the market, and they are no slouches, either. The Mars 432 from Numerix Corp., a young Newton, Mass., company, performs at 30 megaflops and is priced at about \$100,000. Star Technologies Inc., Portland, sells its Star-100, rated at 100 megaflops, for \$250,000 and up. Analogic achieves 9 megaflops with its AP500 processor, which includes local intelligence in the form of a 68000 microprocessor and is priced from \$25,000. Despite their impressive performances, the 32-bit machines are generally considered limited to special-purpose applications such as processing medical images or analyzing radar, sonar, or seismic echoes.

The new 64-bit machines, however, can perform simulation and modeling for three-dimensional weather data or oil and gas reservoirs, heretofore the domain of supercomputers. The reason is that rounding errors in single-precision 32-bit arithmetic will skew results enough to make them meaningless in large calculations, explains Floating Point's Harte. A 32-bit processor can perform double-precision arithmetic in software, but at the expense of performance; each double-precision operation will require four times as many operations as a single-precision operation.

The 64-bit applications



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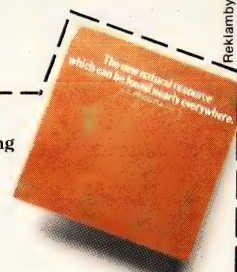


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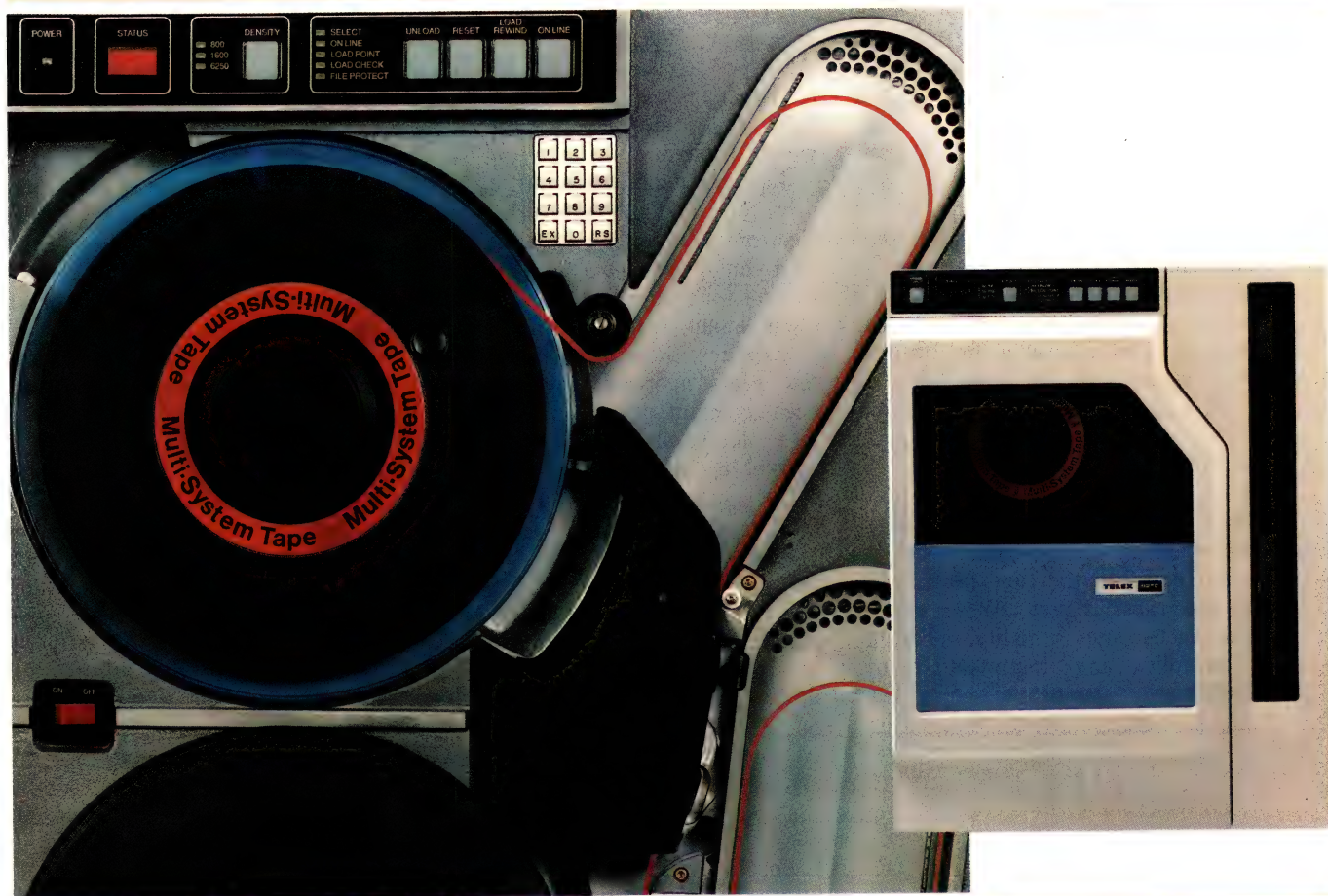
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The HP 7475A quickly "makes friends" with most of the personal computers you may already have in your office, including IBM®, Apple™, Compaq™, Osborne®, and Commodore™—as well as a host of HP computers. You even have a choice of many off-the-shelf software packages that give you "first-day" productivity with the HP 7475A.

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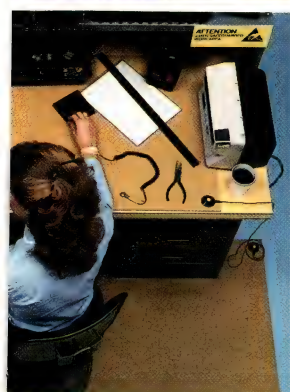
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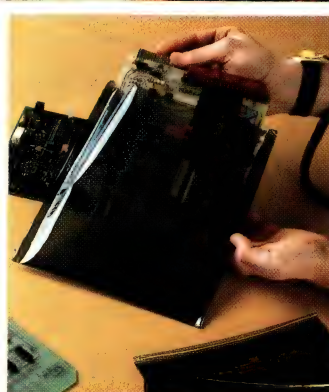




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# COMPUTER GRAPHICS

**Swinging into computing's mainstream, affordable graphics capability springs from powerful, cost-effective hardware plus better software, heightening accessibility of systems and opening up new applications**

by Tom Manuel, *Senior Editor, Information Systems*

□ Computer graphics, one of the key ways in which people can easily communicate with computers, has moved into the mainstream of computing. The reason is its new affordability, largely brought about by the chip-technology advances that are fueling so many other computer revolutions.

Computer graphics can be defined most simply as drawing pictures and charts with computers and is one of the features that many computer users now expect. In fact, it is fast becoming common in present-day computers because of the much lower costs. Professional-quality high-performance graphics is beginning to revolutionize the ease with which more people can enter the computer age. Recognition of this need to make computers easier for the vast number of new users has spurred the development of graphics-based user interfaces.

In business, communicating with graphics has long been recognized as a very efficient means of conveying complex information. It will be even more efficient when professional workers can create such graphics themselves on a personal computer. Computer graphics is also used in computer-aided design.

The driving force behind growth in graphics is primarily the steeply dropping prices and increasing performance of computing and memory resources. High performance in graphics, in both speed and resolution, requires a lot of these resources. Until now, professional-quality computer-graphics systems were too expensive for general use. But now, as 256-K memory chips, second-generation 16-bit microprocessors, and the first 32-bit micro-



## SPECIAL REPORT

processors are coming on stream, the dawn of affordable computer graphics is definitely here.

Also making strong contributions to the increased use of computer graphics are new chips, such as off-the-shelf graphics and video coprocessors, semicustom graphics engines, and full-custom or application-specific integrated circuits, which are much easier to make because of the advances in design tools for application-specific ICs. Moreover, these new design systems are in turn possible in part because of the technical advances

achieved in computer graphics.

Better communications is one of the keys to increased productivity, which is of great interest of industries and businesses everywhere, so it is no wonder that graphics is a hot topic. Because computers are seen as productivity tools, using them to enhance all graphics communications, as well as applying graphics techniques to improve the communication of otherwise dull computer-generated information, is a natural step.

Just three or four years ago, people in computer-graphics companies, like pioneering Tektronix Inc. of Beaverton, Ore., were often asked: "Why are you in computer graphics? It's just on the fringe of the computer industry." That is no longer the case, reports Jon S. Reed, vice president and general manager of the Tektronix Information Display Group. "Large general-purpose-computer companies have recently moved into graphics as graphics companies like Tektronix are putting more computer intelligence into their products," he says.

Computer graphics is going to disappear, according to



along with the basic input/output system in read-only memory, the system RAM, and the other I/O elements; the special processors—a graphics coprocessor and a display processor—and the graphics display memory (frame buffer) are on a separate 16-bit graphics bus.

As the roster of other present offerings suggests, most if not all general-purpose computers of all sizes will sport high-performance graphics. Examples of such systems, in addition to the Mindset personal computer, include Syte Information Technology Inc., San Diego, with its 32-bit series 3000 networked computer; the Ridge 32 series of single-user and multiuser, reduced-instruction-set mainframes from Ridge Computers, Santa Clara, Calif.; the Domain systems from Apollo Computer Inc., Chelmsford, Mass.; the Perq networked systems from Perq Systems Corp., Pittsburgh, Pa.; and the Masscomp WorkStation 500 computer from the Massachusetts Computer Corp., Westford, Mass.

### Working on resolution

Resolution has been and still is one of the big technical challenges in graphics. There are two issues involved. First, there is the question of how much resolution is required within the computer to represent and manipulate the information being graphed. Second, there is the question of how much resolution is needed on the output medium—display or hard copy. The resolution required is usually different in these two areas—sometimes less is required inside the machine than in the output—but, for some applications, more picture elements are stored and manipulated than are displayed, for example in electronic-publishing applications where character fonts and other information are stored in the bit map but don't appear on the display. The output-resolution requirements differ for different display and hard-copy devices, depending upon the intended use of the output and the technical capabilities of the device.

High resolution costs money—in the processing and memory hardware to store and manipulate all the pixels, as well as in display and hard-copy output devices. If ways can be found to get crisp, bright pictures in many colors on a display while keeping the internal resolution to no more than is required for accurate representation, these may be better solutions than a brute-force increase of resolution throughout the system.

Several techniques have been developed to reduce aliasing (commonly known as the jaggies), which appears on raster-scan lines and curves at angles to the vertical and horizontal. Most employ some method of selectively brightening or enlarging the spots (pixels) to produce an apparently smoother line. Unfortunately, these techniques tend to give the overall display a fuzzy or unfocused appearance.

One company, Megatek Corp. of San Diego, has developed and patented an antialiasing technique that repositions the pixels by small amounts, vertically or horizontally, as they are being displayed. Megatek calls its process pixel phasing. (The technical details of pixel phasing are presented in an article beginning on page 118.) Other graphics companies are meeting higher-reso-



**2. Plot in color.** Personal computers, as well as bigger machines, can plot color output on paper and transparent acetate with low-cost plotters like this HP 7550A. Since it is fast and has an automatic cut-sheet feeder, this plotter can be a central plotting resource.

lution color-display requirements by straightforward increases in raster resolution or through the development of color calligraphic (vector refresh) displays, where complete vectors are drawn from end-point coordinates, such as the work stations from Evans & Sutherland Computer Corp., Salt Lake City, Utah.

Within the last year, flicker-free color raster-scan displays with 1,280 by 1,024 or 1,024 by 1,024 pixels, refreshing at 60 hertz, noninterlaced, have become available from all of the high-end graphics terminal suppliers. They look good and are all pretty much alike. By and large, they are driven by powerful graphics processors providing fast picture changes. This level of graphics performance has become standard for CAD/CAM systems and for the newer computer-aided-engineering systems. The many personal computers with graphics display capability, however, have lower resolution—in most cases today, much lower resolution.

A different approach to resolution has been taken by Lexidata Corp., Billerica, Mass., in the LEX 90 family of raster-display and graphics systems (see p. 171). One of the features of this new system is a simultaneous dual-resolution capability Lexidata calls SimulRes. For example, a shaded solid image at a resolution of 640 by 512 pixels can be displayed beside a wire-frame image (where the object is displayed as a series of line segments outlining its surface) having a resolution of 1,280 by 1,024 pixels.

Perhaps a resolution of 1,280 by 1,024 pixels is enough for many applications. Even lower internal resolution



adding quality graphics to low-cost systems.

Among standard graphics ICs is the EF 9367 display processor from Thomson—EFCIS, Grenoble, France. A chip set consisting of the 7300 color-graphics controller and the 7301 memory-interface controller comes from NCR Corp.'s Microelectronics division in Colorado Springs, Colo. [*Electronics*, April 19, 1984, p. 166]. Another, from Xtar Electronics Inc., of Elk Grove Village, Ill., consists of a graphics microprocessor and a video shift register [*Electronics*, May 3, 1984, p. 184].

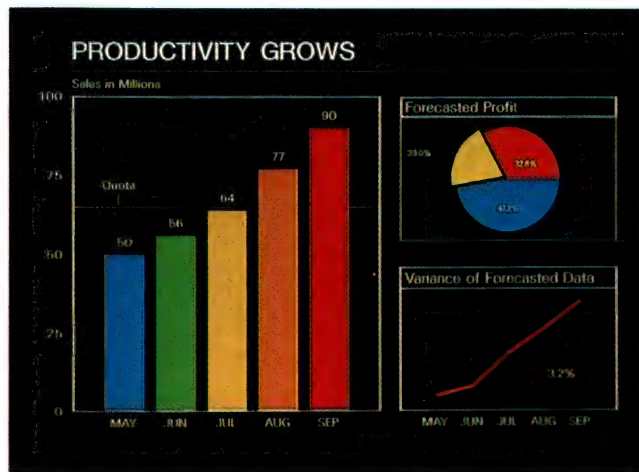
Joining the list of graphics-board products is the iSBC 186/78 video graphics subsystem from Intel. It integrates an 80186 CPU with a 82720 graphics controller, display memory, a buffer, shift registers, color-lookup table, and a multibus interface. The 186/78 is a programmable subsystem that can completely handle medium-resolution graphics—monochrome or color raster at a display resolution of 1,024 by 800 pixels by 1 plane or 512 by 512 pixels by 4 planes for 16 simultaneous colors out of a palette of 4,096. The 186/78 can be programmed by the user or can run graphics software from Intel—two packages currently available are iPLP720, for the Naplps (North American Presentation-Level Protocol Syntax) standard from the American National Standards Institute and the Canadian Standards Association, and iVDI720 for the ANSI VDI (Virtual Device Interface) standard.

### Getting hard copy

In cases where hard-copy output from computer-graphics systems is for presentations, the resolution requirements are greater than for display. Very high-resolution film recorders for the highest-quality output have been available for a while. Recently, suppliers such as Polaroid Corp., Cambridge, Mass.; Matrix Instruments Inc., Orangeburg, N. Y.; and Image Resource Corp., Westlake Village, Calif., have introduced low-cost cameras for producing transparencies and prints with resolutions up to 4,000 lines. For example, the Samurai system by Image Resource is priced under \$10,000 [*Electronics*, May 3, 1984, p. 192].

However, there is a big demand for high-quality color hard copy on paper at lower costs than these film recorders. Even if color printers, copiers, and plotters cost about what film recorders do, the cost per copy will be less. Fortunately, some color devices arriving on the market produce high-quality color hard copy yet cost well below \$10,000. Multiple-pen plotters and color ink-jet copiers are two of the technologies now being employed and constantly being improved.

HP's San Diego division is now working with multipen color plotters and has a product line on the market. The most recent model (Fig. 2) is the HP 7550A at \$3,900 [*Electronics*, April 5, 1984, p. 190]. Another multipen color plotter available is the Sweet-P from Enter Computer Inc., San Diego, at \$1,095 [*Electronics*, Dec. 15, 1983, p. 177]. Tektronix is into color hard copy with its air-assisted, drop-on-demand ink-jet technology. It will extend its product line of color ink-jet copiers with a new model this summer. Xerox' Versatec Co., Santa Clara, developed the first electrostatic color plotter. It can plot



**4. The ultimate.** For the highest resolution and the most saturated colors, film image recorders do the best job today. This reproduction is of a 35-mm slide from a recorder driven by the Tell-a-graf software package from Integrated Software Systems Corp.

E-size (34-by-42-inch) drawings in minutes.

Black and white plotters and printers also have been increasing in resolution while dropping in price. For example, Imagen Corp., Mountain View, Calif., has introduced both 480- and 300-dot/in. laser printers at \$20,000 and \$9,950, respectively [*Electronics*, May 31, 1984, p. 116]. Benson Inc., San Jose, and Versatec both unveiled high-resolution electrostatic plotters at the Computer Graphics '84 conference. Benson showed its 9800 series with a writing head containing four offset rows of styluses rather than the usual single or double row. The resolution of 508 dots/in. gives plots that look like quality pen-and-ink drawings. Versatec's new 7000 series has a plotting resolution of 400 dots/in.

None of the great displays, phenomenal-resolution hard-copy devices, or the fast graphics-processing engines are of any use at all without software to produce the final result (Fig. 3). Progress in graphics application software with simple user interfaces has been significant in the past year. Also, much progress has been made in setting and adopting standards for the software for basic graphics functions—the International Standards Organization/ANSI GKS (Graphics Kernel Standard) for graphics primitives, for example—and device-independent output routines—such as the VDI and Naplps standards.

An example of what one of the high-level user-oriented graphics application packages can deliver in conjunction with a film recorder is shown in Fig. 4, which was reproduced from a 35-millimeter slide produced by the Tell-a-graf package—version 5 with layout intelligence—from Integrated Software Systems Corp., San Diego. Other equally capable graphics application packages are available from such companies as Precision Visuals Inc., Boulder, Colo.; Graphics Software Systems Inc., Wilsonville, Ore.; Brag Systems, San Mateo, Calif.; Apple Computer Inc., Cupertino, Calif.; Mindset; Digital Research Inc., Pacific Grove, Calif.; Visual Engineering, Davis, Calif.; European Software Contractors A/S, Copenhagen, Denmark; and others. □

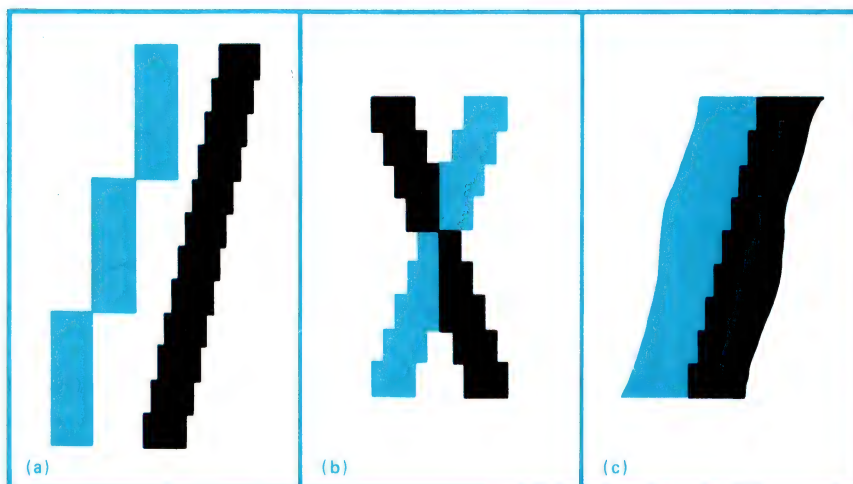


**2. Horizontal phasing.** Pixel phasing can also remove jaggies from lines that are close to the vertical axis. In this case, the pixels can be shifted horizontally in  $\frac{1}{4}$ -pixel increments by changing the raster scan's phase for successive pixels.

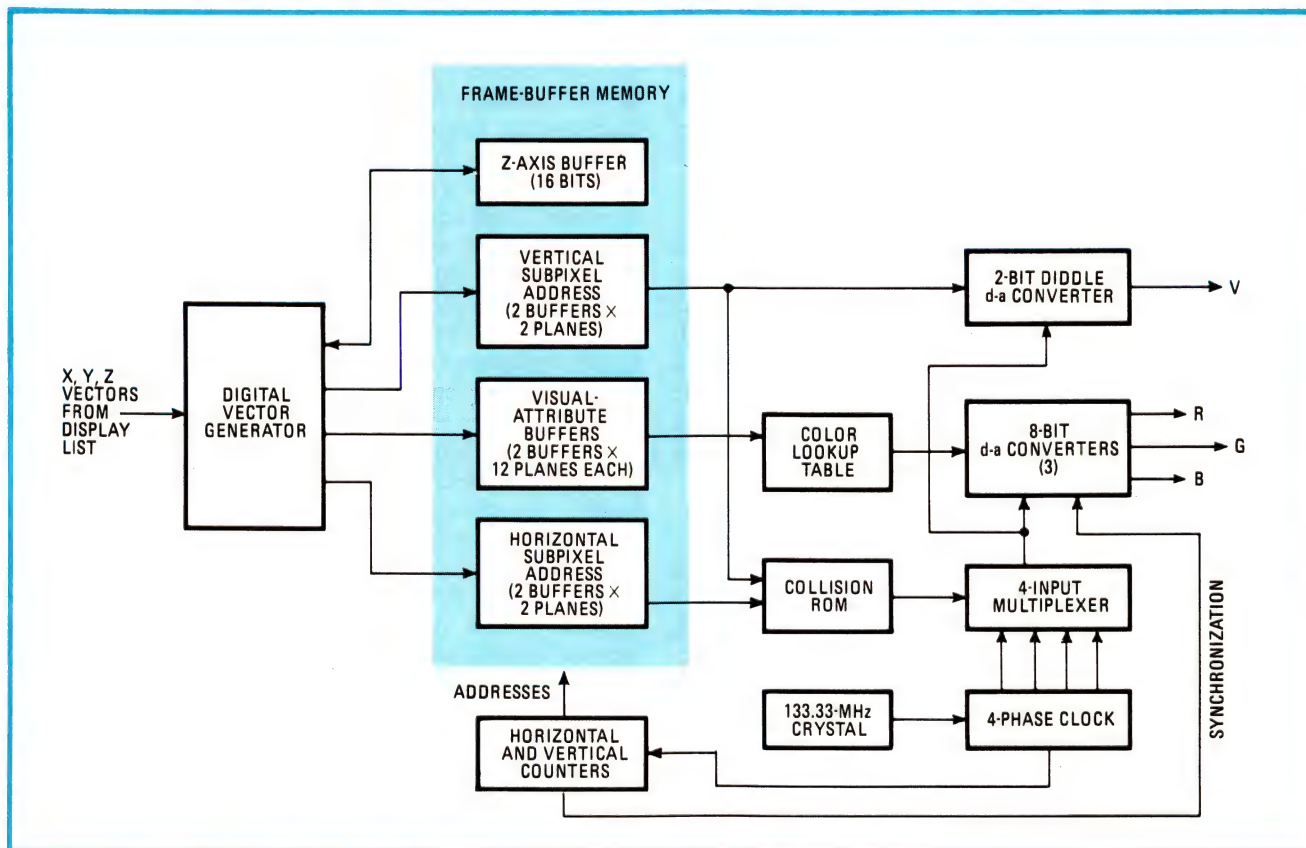
multaneously displacing the left and right pixel boundaries in  $\frac{1}{4}$ -pixel increments reduces the jaggies. Boundary displacement also works on intersecting lines (Fig. 2b) and between pixels of two solid areas (Fig 2c).

The output section of a conventional raster-graphics engine contains a digital vector generator, a frame-buffer memory, a color-lookup table, d-a converters, and control circuits. Pixel phasing is added by modifying the digital vector generator, including four extra bit planes per buffer within the frame-buffer memory, and generating a four-phase clock to enter data into the d-a converters. The four extra bit planes store subpixel addresses for both axes—2 bits for X-axis phasing and 2 bits for Y-axis diddling.

In the output-section architecture with pixel phasing in Figure 3, vector end points (X, Y, Z) from the display list are entered into the digital vector generator, which



interpolates (X, Y) pixel addresses in a conventional manner. Subject to comparison with data from the Z-buffer, the pixels are written into a 12-plane read/write visual-attribute buffer. As the digital vector generator proceeds along the major axis, it creates an extra 2 bits of precision (the subpixel address) to indicate more accurately the location of pixels along the minor axis. These extra 2 bits are stored in the vertical or the horizontal subpixel address planes of the frame-buffer memory, depending upon whether the major axis is X or Y. For



**3. Sub-pixel addressing.** The circuitry needed to do the subpixel addressing required for pixel phasing is little more than the typical output section of a graphics engine. Two planes of frame-buffer memory are added for each vertical subpixel and horizontal subpixel address. A collision read-only memory and a multiplexer are also needed.





# A new-generation video processor boosts resolution

Chip also has modes that operate autonomously from the system host

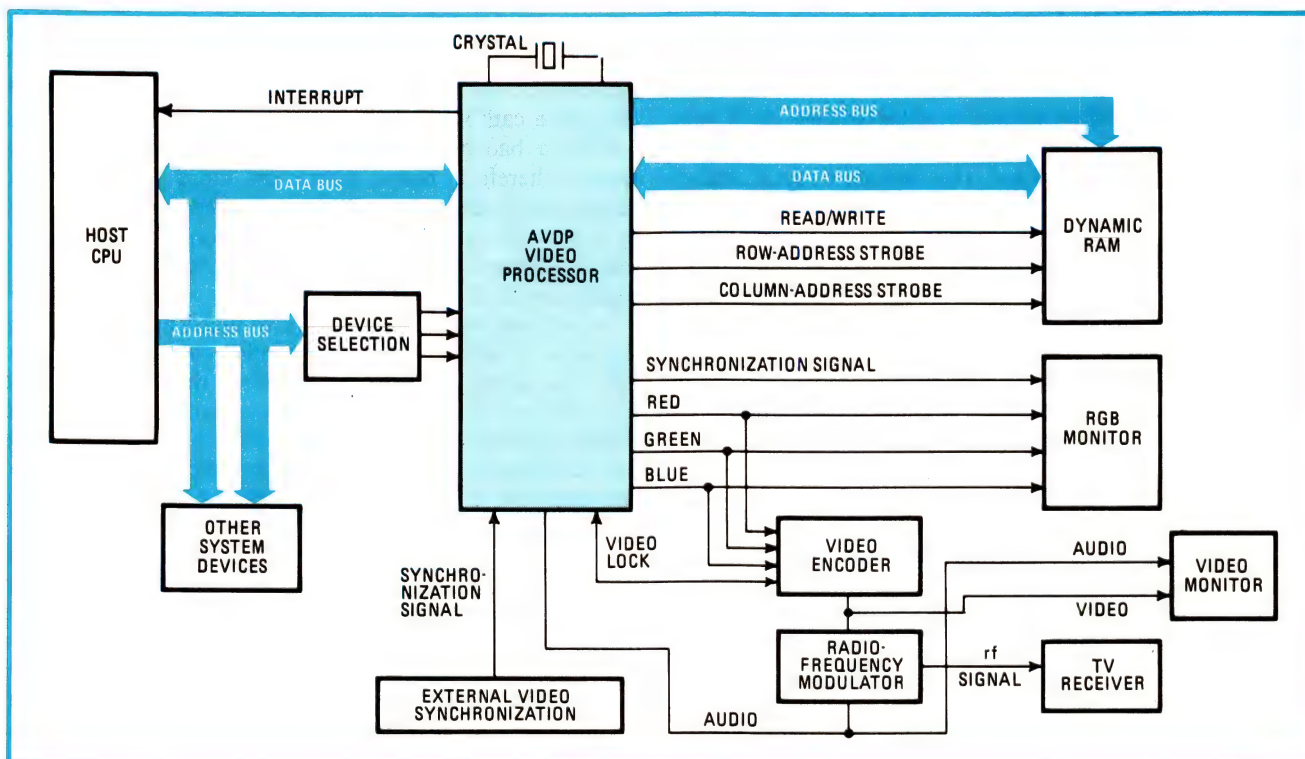
by Mark Kisner and Jean Ladd,  
Texas Instruments Inc., Houston, Texas

□ New video-display processors are playing an important role in dropping the cost of applications with complex display requirements. Personal computers, office terminals, industrial and medical instruments, information systems, educational equipment based on video disks, and entertainment gear collectively represent merely the tip of the application iceberg for enhanced but inexpensive video-display processing.

Aiming at meeting that demand, one member of a new family of advanced video-display processors from Texas Instruments—the AVDP (Fig. 1)—meets all North American Presentation-Level Protocol Syntax (Naplps) standards. Indeed, the video processor goes beyond Naplps' basic requirements and offers many additional functions:

40- or 80-column color text, smooth horizontal and vertical scrolling, the overlaying of conventional video with alphanumeric and graphics symbols, table-driven graphics, complex sprites for enhanced animation, a block-moving capability, direct memory access by the host computer to the video memory, a complex sound generator, software color selection, and more. The ADVP also has a very high resolution compatible with the U. S. domestic (NTSC) television standards, and another version is compatible with Europe's PAL systems.

Of course, the video processor must have appropriate interfaces, all of them built into the two AVDP configurations, which fit into a 40- or 48-pin dual in-line package. First, the video processor provides a general-purpose in-



**1. Interfaces.** A new video display processor goes beyond the requirements of the North American Presentation Level Protocol Syntax standard. For example, by using the synchronization port, external video can be overlayed with images or text stored in the processor.



**3. Sprites.** Up to 32 sprites—special hardware-generated images—can be displayed at the same time. Each sprite can be in a different plane with different priorities. Background, pattern, and external video planes can also be displayed with the sprite planes.

or the soil. In addition, perhaps four or five lines of text could be placed at the bottom of the scene.

Besides all these scene enhancements and animation devices, background scenery and objects can be smoothly scrolled up and down or side to side, slowly or rapidly and in a way that is very pleasing to the eye. In the text mode, as well, pages can be scrolled up or down, and parts of a page can be moved for text insertion. Text can also be set in a standard color contrasting with the background, or several colors can be used—for example, to highlight misspelled words in a special color or to underline words in another one, or even to cause certain sections of the text or scene to blink on the screen.

### Inside the chip

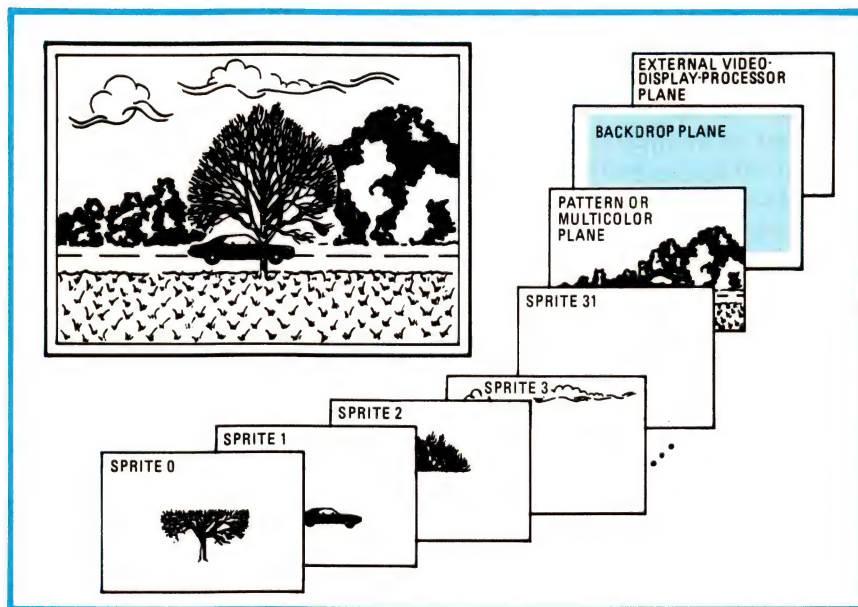
Inside the chip are a host of integrated functions (Fig. 2). Starting at the video processor's interface with the CPU, there are an 8-bit bidirectional data bus, three control lines generally derived from the host's address output, and an interrupt line. The three control lines must be decoded by external device-selection logic. Although each host microprocessor generally requires individual adaptation, most adaptations can be accommodated rather easily.

No adaptation is needed to control standard dynamic-RAM configurations. The video processor provides the refresh control directly with standard RAS, CAS, and R/W signals and an address and a data bus.

The memory accompanying the AVDP chip can have several configurations. The video processor can handle 16-, 32-, or 64-kilobyte dynamic-RAM arrangements directly. For example, two 16-K-by-4-bit dynamic RAMs can provide 16 kilobytes of memory and four can supply 32 kilobytes. Eight 64-K-by-1-bit memories will give 64 kilobytes, and two of the new 64-K-by-4-bit memories are enough for the 64-kilobyte configuration.

The processor can handle even more memory if the host microprocessor chooses among several memory banks that the video processor can then address. In fact, paging can be arranged so that one memory bank provides low resolution—for instance, only 12 kilobytes for rapid animation—and the others have larger memory spaces for high resolution. The display could then page through successive scenes while updating scenes not displayed at that time.

Should a scene with animated sprites be on screen, one of the video processor's functions is to keep track of



colliding sprites, which are very important in video games. In such applications, the video processor makes it unnecessary for the CPU to remember, say, when a killer-rocket sprite has zapped a spaceship sprite.

The 32 sprites are arranged into eight groups. When a sprite collision occurs, it is recorded in one of the sprite processor's registers, so the CPU learns about the event. Because of the register's size—8 bits—and its eight-group arrangement, the sprite processor can detect collisions among eight unique sprite groups in one event.

Making sprites collide is easy. Since sprite coordinates are defined precisely by their picture-element coordinates, sprites can be moved and positioned very accurately. They are available in such sizes as 8-by-8, 16-by-16, and 32-by-32 pixels.

### Keeping track

While the collision mayhem is occurring, the background scene—controlled by the video processor's horizontal and vertical counters—can be scrolled in any direction. Eight-bit horizontal and vertical scroll registers can supply an address offset to the respective counters to change (on the display) the address and thus the location of the initial fetch of the scan lines from the dynamic RAM. From 1 to 256 pixels can be scrolled at once, so control is very smooth. Similarly, three registers and associated counters control the block-moving function for both the text and the graphics mode.

A priority-and-attribute controller circuit establishes a set of overall display priorities: first the sprites are shown (if any should be called for) and then the priority of their appearance is determined. In the absence of sprites, the basic graphics or text-pattern plane is displayed. Should the pattern plane be transparent, the external video (if any) appears on screen.

In other words, the display may be envisioned as a set of display planes, arranged in a hierarchical fashion, one atop the other (Fig. 3). The sprites, objects, or planes



# A few statement types adapt C language to parallel processing

Adding process-synchronization and -communications facilities gives enhanced hardware flexibility, faster computation, and more power

by Ray Naeini, *Flexible Computer Corp., Dallas, Texas*

□ Building on the success of the C programming language in conventional sequential-processing environments, ConCurrent C is designed for concurrent and real-time processing on multiple-processor systems. It was created as a production software-development tool for computers that process multiple instruction streams operating on multiple data streams (see "Multicomputing hardware epitomizes flexibility," below).

ConCurrent C preserves all of the definitions and features of C, so that the standard language is upward-compatible with ConCurrent C. The aim was to provide simple, structured, C-like syntax with a minimal number of new key words; the extensions offer generic capabilities for the implementation of a wide variety of programming concepts. In other words, ConCurrent C provides mechanisms without dictating techniques.

The new key words and statement types support real-time event supervision and concurrent processing on multiprocessor systems, as well as the usual sequential

environments. Additional language features can be obtained by combining those provided by ConCurrent C with various programming techniques and styles. Its simple, generic capabilities make the new language adaptable to new hardware and applications.

Concurrent processing with multiple processors is a technique for achieving more processing power, faster computation, and flexible application of hardware to changing requirements. The term concurrency, however, has come to have more than one meaning. It is often applied to what might be called "apparent" concurrency: that is, a number of processes sharing a single processor, slicing up its time among them. A less ambiguous term for this type of operation is multitasking, sometimes called multiprogramming.

"True" concurrency refers to multiprocessing, wherein a collection of sequential processes execute on separate processors. The activities of the processes are in fact carried out at the same instant in time. Combining both

## Multicomputing hardware epitomizes flexibility

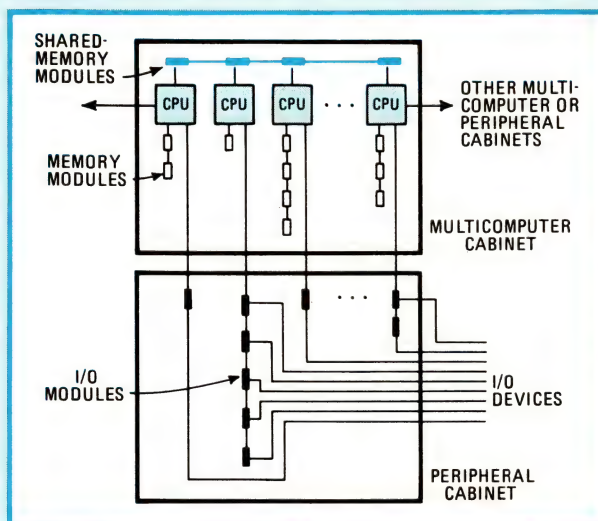
Although the ConCurrent C programming language is intended to serve as a code-development tool for multiple-processor systems in general, the original impetus was the development of the Flex/32 MultiComputer. This system is a collection of independent, self-contained processors that share a common set of interprocessor communication and synchronization facilities and fully arbitrated, high-speed common memory, among other resources (see figure). It executes multiple instruction streams operating on multiple data streams.

Designed to use 32-bit microprocessors as engines, the Flex/32 hardware can be reconfigured easily; thus the system can expand in power with minimal software modification. It can support a mix of up to 20 processors or 160 megabytes of memory in 20 modules.

The computers in the Flex/32 can communicate by shared memory, messaging, or networking; the most common method is through mailboxes in common memory. Communication through what are known as conditional critical regions uses arbitration hardware that eliminates software overhead to improve performance.

The complete system is packaged in a series of cabinets,

some housing the computers and others for peripheral devices. As many cabinets as needed may be linked to create large configurations.





executed. Control then returns to the statement immediately following the one that was performed when the event occurred. For example, an interrupt could be enabled for some part of a program and an interrupt handler written for execution when the interrupt occurs.

In general, for multiprocessing and real-time programming, a language must support:

- Protected access to shared data, to prevent a process from using data while another process is doing so.
- Interprocess communication and synchronization, regardless of the physical location of the processes.
- Creation and concurrent execution of processes.
- Event definition and supervision that allows events to be used as efficient inter- and intraprocess synchronization tools, as well as for response to real-time incidents.

### Event variables

The new constructs in ConCurrent C consist of two classes. New variable definitions include event variables and shared variables, and new control-flow statements apply to process interaction, process control, concurrent execution, and event supervision.

As all real-time events are either timers or exceptions, these event variables are declared and defined by the key words **Timer** and **Exception**. A timer triggers an event when it has counted down from its initial value to some predetermined value, including zero. After a value is assigned to a timer variable, a new statement called **Activate** initiates the countdown. (**Activate** can also update the value of a running timer so that it will continue counting down from a new value.)

A timer is a simple variable preceded by the key word **Timer**. The definition might appear as follows:

```
timer x_time=30;
```

The value of the timer, which is expressed in time units whose length is determined by the implementation environment, need not be defined immediately, however. A construct called **Cyclic Timer** can be used if a timer that will restart automatically after reaching zero is required.

The **Activate** statement can be used to set off an event, either a timer or an exception, thus:

```
activate (x_time);
```

A timer can be killed by setting the variable's value to zero and activating it:

```
x_time=0;
activate (x_time);
```

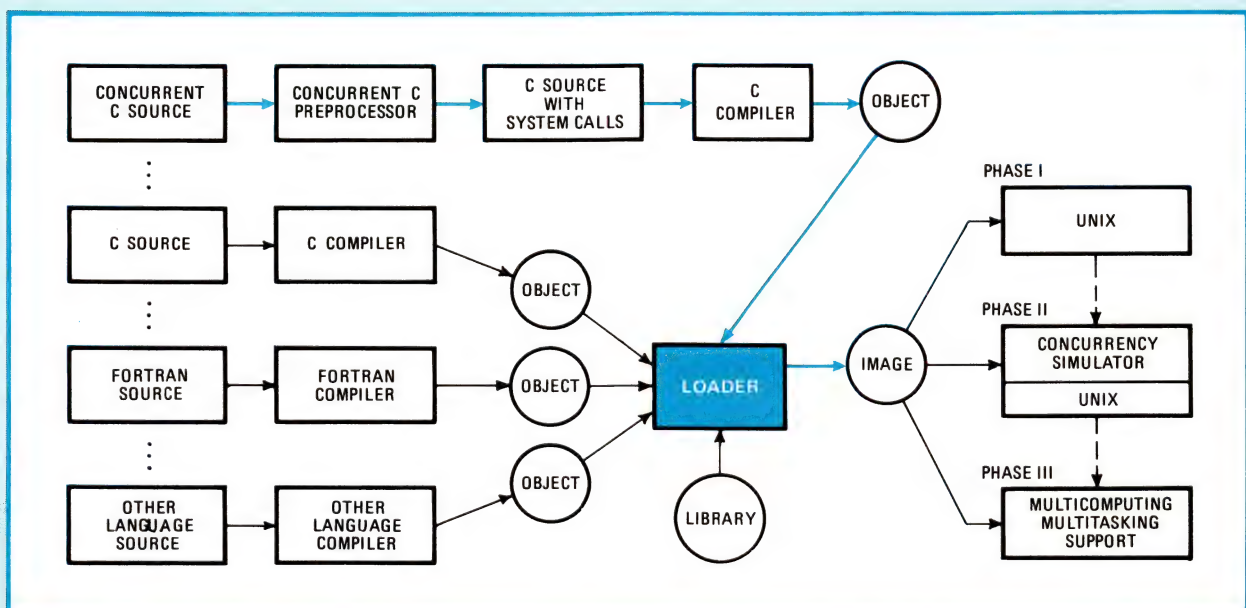
The only identifier required for the **Activate** statement is the event identifier, which must have been defined as a timer or an exception.

### Traps and interrupts

An exception can cause incidents that affect either its defining process (internal exceptions, or traps) or a separate process (external exceptions, or interrupts). Exception variables are treated as Boolean variables (in C, simple integers). An exception that has not been activated has an associated variable whose value is false (logic 0); activation changes it to true (logic 1). The value will be reset to false after the variable has been tested; other-

The software-design team has the choice of compiling other processes written in other languages with the appropriate compilers and combining them with the system load-

er. Once the loader resolves the processes' system calls, the processes can execute together under any of the environments provided.





on the same processor in a multitasking arrangement. Shared variables that are used by processes on different processors are placed in common memory; such variables are therefore static and global by nature.

Shared variables must be locked before being used by a process if valid data is to be assumed. The shared data is protected until the process has finished with it and placed it in a known state again. The process can then unlock the shared data object. Another process attempting to access the locked variable is delayed until the variable becomes available. The period during which a process owns a shared variable and operates on it under lock protection is called a critical region.

### Identifying shared variables

No new key words need be defined to identify shared variables. Standard C's external and external-static variables define appropriate scopes for shared variables and can make them known to specific processes. Any external or external-static variables that are shared between processes (rather than by just the functions within one process) are implicitly considered to be shared variables.

The conditional-critical-region technique can use the When and When-Else statements for interprocess synchronization. Each process will be delayed until the defined condition is satisfied; this constitutes conditional synchronization. When the condition is satisfied, the process will be allowed to execute a set of statements known as the critical statements. Exclusive use of critical shared data—mutual exclusion—is guaranteed during this time, and the entire operation in the critical region will appear as an indivisible operation to other associated processes.

For instance, a shared buffer, called Buffer, might be used by process p1 to write data, and by process p2 to read the same data. Another shared variable, Buffer\_status, is used to help synchronize the two processes. With the following code for writing and reading the data into and from the buffer, the protection of the shared variables is guaranteed. Both processes check the status of the buffer for synchronization:

```
/* In process p1: */
when (buffer_status == EMPTY) {
    write_buffer();
    buffer_status = FULL;
}
/* And in process p2: */
when (buffer_status == FULL) {
    read_buffer();
    buffer_status = EMPTY;
}
```

Each When statement block above is equivalent to a sequence consisting of Lock and If statements, a series of critical statements, and an Unlock statement. The When statement combines protection and synchronization into a single statement, automatically generating the Lock, Unlock, and condition-evaluation statements. It hides from the programmer all of the operations required for process suspension and resumption if the locks are not

available or the condition is not satisfied. Lower-level statements (such as Lock and Unlock) are available to the programmer as system calls for direct programming.

The concept of a process is fundamental to multiple-processor programming. In ConCurrent C, a process is defined and started by a Process statement, which includes a unique identifier, the code used by the process for execution, and, optionally, the processor that is to execute it and the system-dependent attributes that define its environment, such as priority and stack size.

System-dependent attributes, if required, are placed in a predefined structure and passed to the system-support environment. This structure can be customized for different implementations or omitted altogether. The process code can be any C function defined in the program text.

The process identifier is defined as an integer and is assigned a value by the system during the execution of the Process statement; thus processes can be created dynamically. The statement can pass new argument values to the function that defines the process body.

### Parent and child

The process started by the Process statement is considered the child process, and the process that is executing the statement is the parent process. This conventional topology retains simplicity and gives complete control over multiple child processes executed concurrently.

The Cobegin control-flow statement provides a joining structure for concurrent execution of processes. The statements defined inside a Cobegin block are executed in the order shown in the block, and the statement immediately after the block will not execute until all processes begun within the block are completed:

```
cobegin {
    process (p1, func1(), processor1);
    process (p2, func2(arg1), processor2);
    process (p3, func3(), processor2);
    <statements> /* handled by parent process */
    process (p4, func4()); /* default processor*/
}
i++;
```

Processes p1, p2, p3, and p4 are started, and the <statements> are executed in the Cobegin block by the parent process. Processes p2 and p3 are executed by the same processor, an example of multitasking. The system loader is forced to decide which processor should execute p4 based on system load and other factors. The i++ statement will not be executed until all processes started within the block have terminated.

If a Process statement is used outside the Cobegin block, the parent process will not be delayed. Parent and child will run at the same time in either true or apparent concurrent fashion.

As an alternative to this method, event-supervision constructs can control concurrent process execution. Exception events can be set up to signal completion of child processes and a When statement can delay execution of the parent until the signals are all received. □



# Denser process gets the most out of bipolar VLSI

To shrink bipolar chips to feature sizes of very large-scale integration, IMOX-S technology implements a series of closely related processing steps

by Phil Downing, Pete Gwozdz, and Bernie New, *Advanced Micro Devices Inc., Sunnyvale, Calif.*

□ Design considerations for new integrated systems range widely, from projecting on-board power consumption to estimating production costs, but the principal benchmarks of performance are the speed and density of individual large-scale integrated circuits. Though significant improvements in system size and capability are nothing new, it is only with the most recent bipolar processing techniques, such as IMOX-S (for ion implantation, oxide isolation with scaling), that the benefits of bipolar speed have come to very large-scale integration (see "Designing high-performance systems with newer, faster processors," below).

## Shrinking size, power use

High-speed IMOX technology, introduced in 1980, has been incorporated into such products as the 2901 bit-slice microprocessor and the 29116 bipolar microprocessor, as well as into various programmable read-only memories and logic chips. When development began on IMOX-S, two principal goals were an improvement in speed and in gate densities: chips produced with it were to be denser, incorporate smaller geometries, and be significantly faster than earlier IMOX parts or other bipolar ICs (see table). At the same time, the designers of the new scaled process wanted to avoid the increase in power level that usually accompanies higher processing speeds, and this they brought off as well.

At first, it may seem impossible to satisfy these usually incompatible requirements. IMOX-S, however, succeeds by

concentrating not only on the primary contributions of each processing step but also on how the successive steps interrelate. These interrelationships—one of the more interesting aspects of the IMOX-S process—work synergistically so that the final process is more than the sum of the individual steps.

Like many other processes, IMOX makes use of oxide isolation for device sizes that are smaller than older, junction-isolation processes could achieve. But the designers of other processes opted for an unwalled-emitter structure that requires extra silicon area (the absence of which would allow the emitter and collector regions to make electrical contact, thus incapacitating the transistor) to isolate the collector and emitter regions.

IMOX instead uses oxide isolation to wall off the transistor's emitter (Fig. 1), eliminating the wasted area found in the unwalled-emitter approach—the field oxide defines three of the emitter's four edges. The direct contribution of oxide isolation to shrinking device size is considerable; when combined with a walled-emitter structure, the result is dramatic.

## Speed, too

Oxide isolation and walled-emitter structures have the advantage of speed, as well as of greater density. Device speeds are faster because some of the capacitances that usually reduce the switching speed have been eliminated through the reduced device area. The collector-to-base capacitance usually accounts for 50% of the total delay

## Designing high-performance systems with newer, faster processors

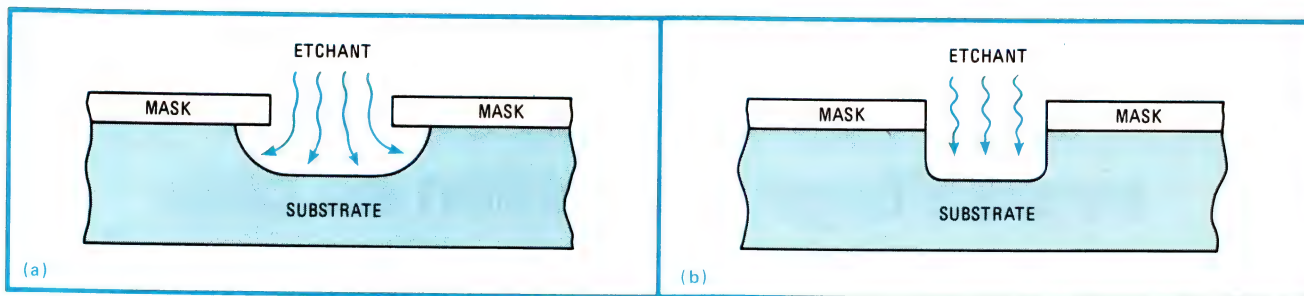
Architectural enhancements such as microprogramming in very large-scale integrated circuits can allow one processor to do more useful work than another in a single instruction cycle—but, as a rule of thumb, the faster a processor executes instructions the better. Hence the single most telling specification for any processor, and potentially the most demanding performance requirement, is the instruction-cycle time.

For pure speed, the 29116A 16-bit microprogrammable processor and the 29517A pipelined 16-by-16-bit multiplier—both fabricated with the IMOX-S process—should be considered for the core of high-performance dedicated

systems such as graphics processors. The 29116A and the 29517A can execute instructions in as little as 80 nanoseconds—more than 10 times as fast as a fixed-instruction-set microprocessor for similar instruction complexity.

Besides the more familiar logical and arithmetic instructions, the 29116A has the type of instructions necessary for image-oriented graphics algorithms. For example, single-clock-cycle instructions can rotate from 1 to 16 places and merge two 16-bit data fields on a bit-by-bit basis, as well as prioritize a 16-bit data value. In addition, the 29517A, through inclusion of pipeline processing, executes a 16-by-16-bit multiplication with a 32-bit result in one clock cycle.





**2. Perpendicular etching.** Isotropic etching (a) removes material in all directions below a mask, making the feature size larger than the limit of the lithographic process. But the anisotropic-etching technique (b) used in IMOX-S burns straight down into the wafer.

(Fig. 3b). The first metal layer can be placed on this planar surface much more reliably and with tighter tolerances, thereby contributing to the overall increase in density.

Smaller metal lines also contribute indirectly to improved performance: if the lines are narrower, because of improved lithography and processing techniques, and shorter, because of higher device density, then the capacitance associated with each line is reduced. Lower capacitance makes higher performance levels possible, especially on high fan-out transistors such as internal output drivers on bus-organized VLSI chips.

Second-layer metal now contends with the newly discontinuous surface introduced by the addition of the first metal layer. A planarization technique called one-to-one etching is used to remove this new discontinuity. The technique first creates an oxide layer over the entire wafer surface, covering metal as well as silicon. A photoresist—which is specially etched at the same rate as the new oxide covering—is spun on with a centrifuge in order to create a smooth surface, and the surface is then etched until only oxide remains.

Because the photoresist etches at the same rate as the oxide, the resulting ox-

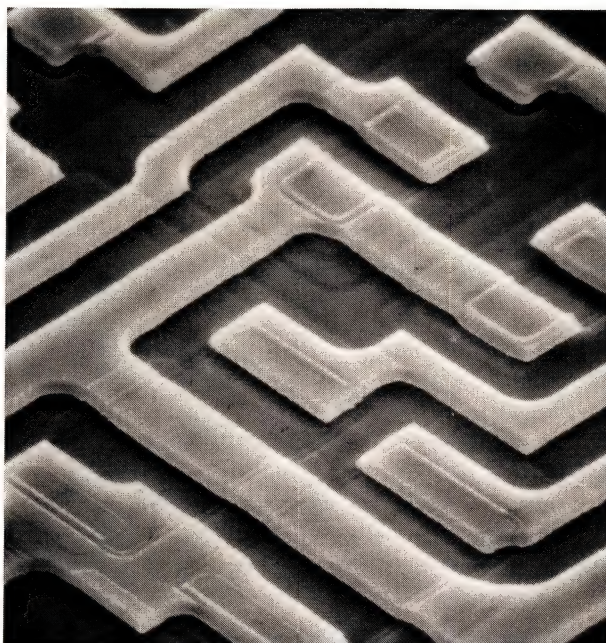
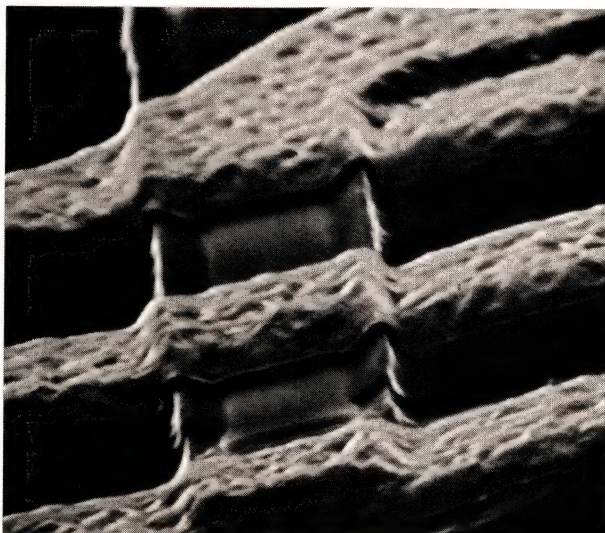
ide surface has the desired smooth planar quality. Hence the second layer of metal has the thin and narrow qualities necessary for a high-density VLSI process.

The third layer of metal in IMOX-S chips is used almost exclusively for power and ground buses—hence a thick, wide metal line is desirable to reduce the resistance of the metal and thus minimize unwanted voltage drops

along these critical lines. A planar surface is no longer necessary after third-layer metal since no critical deposition steps follow.

Owing to the huge commitment of capital and labor for new process development, it is important that an evolutionary path be followed so that it is easy to add future improvements in lithographic and diffusion technologies. IMOX-S can easily use new techniques to further reduce feature sizes because all the critical parameters of its transistor structure can be shrunk or scaled. In fact, the transistor structure was designed with this characteristic in mind.

Further improvements will come with the IMOX X-85 process, with its slot-isolation technique—a narrow groove cut into the surface of the silicon wafer and filled with an insulator to isolate the adjacent active elements. IMOX X-85, now under development, will have a minimum feature size of 1 micrometer and a 2.5- $\mu\text{m}$  metal pitch, meaning that device size can be cut approximately in half. Yet these new devices to be fabricated with IMOX X-85 will deliver twice the performance of those fabricated with the IMOX-S process. □



**3. Smooth.** The first layer of metal interconnection for a conventional bipolar process (a) is much more ragged than in IMOX-S (b). The smoother the silicon and oxide surface below the metal layer, the more reliable the finished integrated circuit will be.



efficient means of controlling power. In fact, smart power ICs rival discrete components in power-control efficiency (Fig. 1).

Smart power has two other important aspects. First, the signal-processing circuitry blends C-MOS and a non-isolated npn-bipolar process; secondly, a variety of output devices are possible. This technology is capable of providing pnp-bipolar, npn-bipolar, n-channel-T-MOS (so named for the T formation of the drain current), conventional silicon-controlled-rectifier, and T-MOS-SCR power outputs. Though the self-isolating nature of C-MOS minimizes the area of any given function, the compatibility between C-MOS and power-device processing maximizes the wafer's yield.

Measuring stress in electronic circuits means measuring voltage, temperature, and current—all of which can be handled by smart power ICs. The bandgap references that are common to monolithic regulators, combined with a simple comparator, will measure voltage quite effectively. Similarly, with the aid of a comparator, these ICs can also measure temperature: the same bandgap circuit that establishes a voltage reference also has well-defined temperature characteristics.

Load-current measurements are equally straightforward. A sample of the current in a series-pass power transistor is taken by adding a diffusion that acts as the collector of a lateral transistor. Since the emitter injects carriers both laterally and vertically, a small  $p^+$  diffusion will act as the collector of a lateral transistor (Fig. 2).

As a result, the transistor produces a lateral current, which is much lower than the vertical collector current: a typical ratio is 1,000 : 1. With such a small amount of current diverted for sensing purposes, the power required is minimal. In fact, this type of measurement is sometimes called lossless current sensing.

For most ICs, measurement is simple, but controlling the input power in a protection application is difficult. This is where smart-power technology excels. The vertical transistors and SCRs that characterize it can handle the power that is encountered in most board-level situations.

The ability of smart-power technology to make superior protection circuits is shown by Motorola's MPC2005, which protects sensitive electronics from overvoltage transients and extreme temperatures. Its distinguishing characteristics are that it is housed in a single package, has a monolithic T-MOS SCR, and offers overtemperature protection and optional control.

As the part is essentially a two-terminal chip enclosed in a TO-220 package, the simple connection of anode and cathode to the appropriate power-supply voltage is required for overvoltage protection. With this

**2. Sensing.** Load-current measurements are made by sampling the current in the output power transistor (a). A small  $p^+$  diffusion acts as the collector of a lateral pnp transistor, which produces the lateral current for sensing (b).

connection, the MPC2005 protects sources with up to 15 amperes of dc output current and 10,000 microfarads of shunt capacitance. The delay time and voltage as well as thermal trip points are set internally. For example, for a 5-volt supply, the delay time is 5 microseconds, the voltage trip point is set at 6.2 v, and the thermal trip point is 125°C. When the device senses any of these fault conditions, it quickly short circuits the supply, thus removing the voltage from the system.

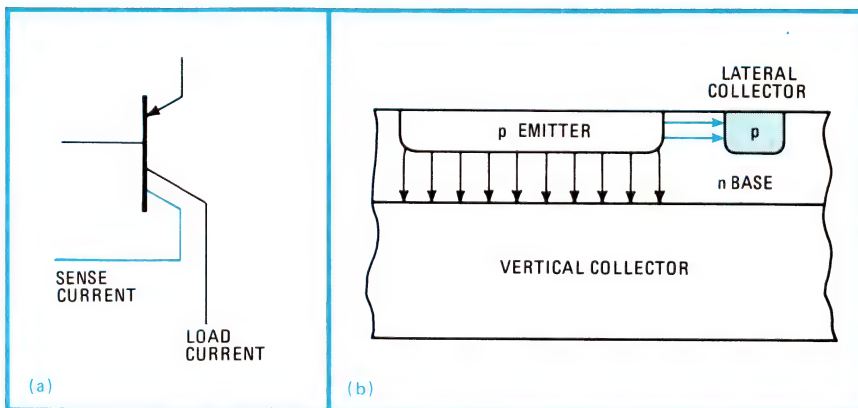
## Bandgap reference

Like monolithic voltage regulators, overvoltage-protection circuits generally use a bandgap circuit to establish the voltage reference. Given the bandgap reference, an overvoltage-protection circuit requires very little additional circuitry to turn it into both an overvoltage- and overtemperature-protection circuit (Fig. 3). Overtemperature triggering is accomplished by relatively few transistors. The connection is such that the output SCR is turned on if either voltage or temperature exceeds the threshold values. Adding the dual function costs little, since the overtemperature circuitry takes up less than 2% of the total die area.

The MPC2005, with its 125°C trip point, primarily monitors power-device heat-sink temperatures. With a lower threshold, overtemperature triggering can also monitor ambient air temperature. Either way, the standby power dissipation of the internal C-MOS circuitry is so small that the on-chip thermal sensing circuitry sees an accurate representation of case temperature. In other words, the heat-sink tab of the TO-220 package, in which the chip is housed, is in effect a temperature-measurement device, whether it is mounted on a heat sink or in free air.

From a design point of view, the most significant technological advance is the integration of a vertical T-MOS SCR with C-MOS control circuitry. The reduction of these components to monolithic form gives ICs their substantial size, weight, complexity, and cost advantages. In addition, the combination of C-MOS logic and a T-MOS SCR boosts performance over a conventional SCR by lowering power consumption, increasing response speed, and ensuring immunity to high rates of change of voltage over time.

An isolation process separates the vertical-SCR structure from the signal-processing circuitry. The T-MOS SCR uses approximately 60% of the die area, with signal-





# ECL-CML gate array speeds superminis while saving space and power

Fast new arrays open the door to denser semicustom circuitry, helping superminicomputers face off the competition from above and below

by Roger Cox, Honeywell Digital Products Center, Colorado Springs, Colo.

□ Traditionally, minicomputer design has relied heavily on Schottky TTL technology, but today, designers are considering emitter-coupled logic to boost the performance of the next generation of machines. Without question, ECL is the fastest logic family available today in production quantities. Its raw speed can certainly help raise the processing power of top-of-the-line minicomputers. What's more, ECL gate arrays combine this speed with density advantages.

But before specific ECL design strategies are considered, it is useful to examine the needs and direction of the superminicomputer market. An understanding of what this market is and where it is going will certainly clarify the hardware-design tasks for the next generation of machines. A careful look at trends in the semiconductor industry shows that designers can best exploit the speed of ECL by using semicustom gate arrays to meet the needs of the evolving superminicomputer market.

Since its introduction, Digital Equipment Corp.'s VAX virtual-memory architecture has set the standard for the 32-bit superminicomputer market. Memory management and protection are now required features, and minicomputers have proved themselves in multiuser applications supporting huge data bases. With these capabilities, minicomputers have been threatening traditional mainframe machines, while they have also begun facing serious challenges from microcomputers using very large-scale integrated circuits. The availability of single-chip, 32-bit virtual machines with performances in the range of 1 million to 2 million instructions per second will certainly put pressure on the low end of the minicomputer market.

To remain competitive, the next generation of superminicomputers must capitalize on the speed and density improvements of ECL large-scale inte-

gration. While ECL is a very fast logic family, nearly all available circuit functions are at a small or medium scale of integration. ECL simply cannot draw on the large library of LSI and bit-slice components that were available with TTL. However, the ECL gate arrays that are available permit the construction of dense, customized circuitry. Gate arrays help designers solve one of the most basic system problems, that of interconnection.

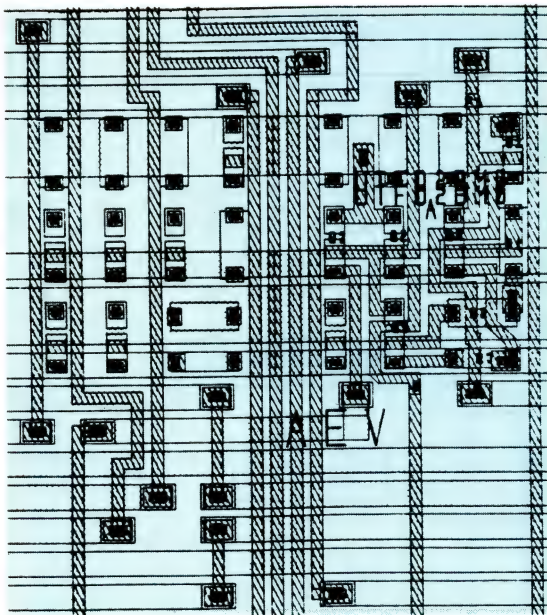
## High-speed interconnections

At moderate speeds, interconnections between chips are minimized for reasons of cost and space. At subnanosecond speeds, they increase power dissipation and add significant propagation delays. Gate arrays minimize these interconnections by placing most of them in silicon.

With the gate array, many advantages of custom circuitry are realized without the traditional expense and delay of a complete IC-development program. In the HE2000 gate array (Fig. 1), with a large array of uncommitted circuit elements, the designer generates two layers of custom metalization to meet specific system requirements. These metal interconnection patterns can be generated rapidly with the proper computer-aided-design tools and a macrocell library.

The macrocell library contains the circuit-connection details to configure a particular cell, or cells, to become a specific logic element. Such logic functions as gates, latches, multiplexers, and flip-flops are commonly available. Using the CAD system, these macrocells can be assembled quickly into a complex system.

The HE2000 is an excellent example of bipolar gate-array technology. It is fabricated using Honeywell's Advanced Digital Bipolar-II process, which is based on oxide isolation, a nonwalled emitter structure, and three layers of metalization.



**1. ECL-compatible gate array.** This portion of the artwork of the HE2000 ECL-CML gate array shows the three layers of metal. Two layers provide customized interconnections, while the third distributes power throughout the array.



tary outputs. The availability of both signals is helpful in minimizing the number of logic functions required on the chip.

The array provides 140 ECL 10K-compatible input/output buffers. Input-receiver circuits translate 10K logic levels to CML levels used inside the array. The logic reference of these input circuits permits them to track the temperature characteristics of the ECL 10K/10KH logic families. As many as 64 of the I/O cells can be configured as outputs. Cells providing ECL-compatible outputs for driving 25- to 80-ohm loads are available. Delay through an I/O cell pair is typically 1.5 ns. The unit is usually mounted in a 173-pin, cavity-down, grid-array package.

### Superminicomputers: the next generation

The next generation of computers with VAX-like architectures offers some intriguing performance possibilities. Some conceivable system specifications are:

- Performance of 10 to 12 MIPS in a single-processor configuration.
- Processor cycle times of 25 ns.
- Main memory up to 32 megabytes.
- High-speed I/O capabilities to support large disks and computer networks using a system-bus bandwidth of 160 megabytes/s.

Subnanosecond ECL-compatible gate arrays and high-speed ECL random-access memories should make such a system possible. Cycle times of 25 ns for a microsequencer with 10-ns access RAMs in its control store are feasible, and data path delays are minimized. In the VAX-11/780 architecture's data paths (Fig. 3), the large number of input multiplexers, output lines, registers, and control lines prohibits the use of a prepackaged bit-slice element. But the HE2000 gate array, with its 140 I/O pins, is certainly advantageous for just this type of application.

This gate array's fast logic can also be used to construct a high-speed register file with a 3-ns access time, much faster than the 10-to-15-ns times available in a standard ECL function. Two distinct gate-array metalization patterns are used in this example—one for the data paths and arithmetic and logic unit and the other for the construction of the high-speed register files. As for comparisons between the gate array's 32-bit look-ahead ALU and that of an equivalent ECL 10181/179 combination, the gate array introduces a worst-case delay in the subtraction mode of 15.5 ns, while the medium-scale ICs give a delay of 29 ns.

The table compares the performance and IC count of three ECL implementations of the described 32-bit data path. The gate-array designs have only a 23-ns worst-case delay from the register files through the ALU and multiplexers and back to the register files, while the 10K MSI and SSI system takes 50 ns. The array implementations also make a significant reduction in system package count, from 208 down to 24 packages.

The advantages of the HE2000 array's CML internal circuitry become more apparent when total power com-

| Circuit technology                            | Number of ICs | Worst-case critical-path delay (ns) | Power dissipation (W) |
|-----------------------------------------------|---------------|-------------------------------------|-----------------------|
| Small- and medium-scale emitter-coupled logic | 208           | 50                                  | 94.2                  |
| ECL gate array                                | 24            | 23                                  | 112.6                 |
| ECL/current-mode-logic gate array             | 24            | 23                                  | 52.0                  |

parisons are made, since the arrays require about half the power of the pure ECL components. It should be noted that when functions are incorporated onto the CML arrays, the emitter-pulldown resistors are eliminated completely from the system; but when ECL is utilized internally on a gate array, the pulldown resistors are still present on the gate-array chip.

Achieving instruction-execution rates in excess of 10 million cycles/s will require more than fast components; extensive pipelining of the instruction stream for fetching, decoding, and execution will be required. The amount of hardware necessary to do this requires a level of complexity that is not found in many of today's superminicomputers.

The Gould Inc. Concept 32/87 is an example of an ECL central processing unit with instruction pipelining. The performance of this machine is impressive, but the price paid in terms of space and power is high when only SSI and MSI parts are used; the 32/87 consists of 18 circuit boards, while the lower-performance 32/57 unit, using TTL circuitry, requires only three.

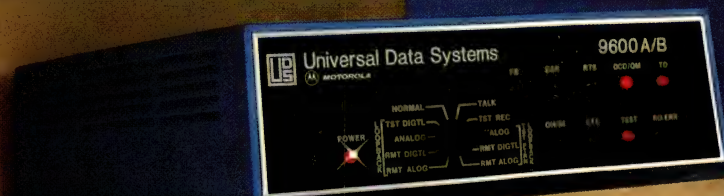
In applications where both speed and hardware complexity are desired, ECL and CML gate arrays will be very helpful in future designs. Any consideration of instruction-pipelining techniques must include the design of a high-performance, closely coupled cache-memory unit. The recent availability of 4-K ECL RAMs with worst-case access times of 10 ns is certain to make the design job easier. These bipolar memory chips are capable of implementing the actual cache as well as the mapper that is required for the virtual-to-physical address translations.

Memory bandwidth must also be increased as CPU performance improves. Increases in system I/O rates seem inevitable for future machines, too, as superminicomputers begin supporting larger complements of disk drives, local networks, and I/O-intensive graphics work stations for CAD, computer-aided engineering, and computer-aided manufacturing.

### Upping reliability

While system-bus bandwidths of 5 to 30 megabytes/s were adequate for the previous generation of machines, the next generation may well require as much as a 160-megabyte/s bus. This 32-bit synchronous bus would have a cycle time of 25 ns and employ ECL signal levels. The memory controller interfacing the bus to the memory chips should support memory interleaving and apply the nibble-mode feature of the new 256-K MOS RAMs. In a block diagram of this design (Fig. 4), showing which areas would use ECL and TTL levels, ECL accounts for all





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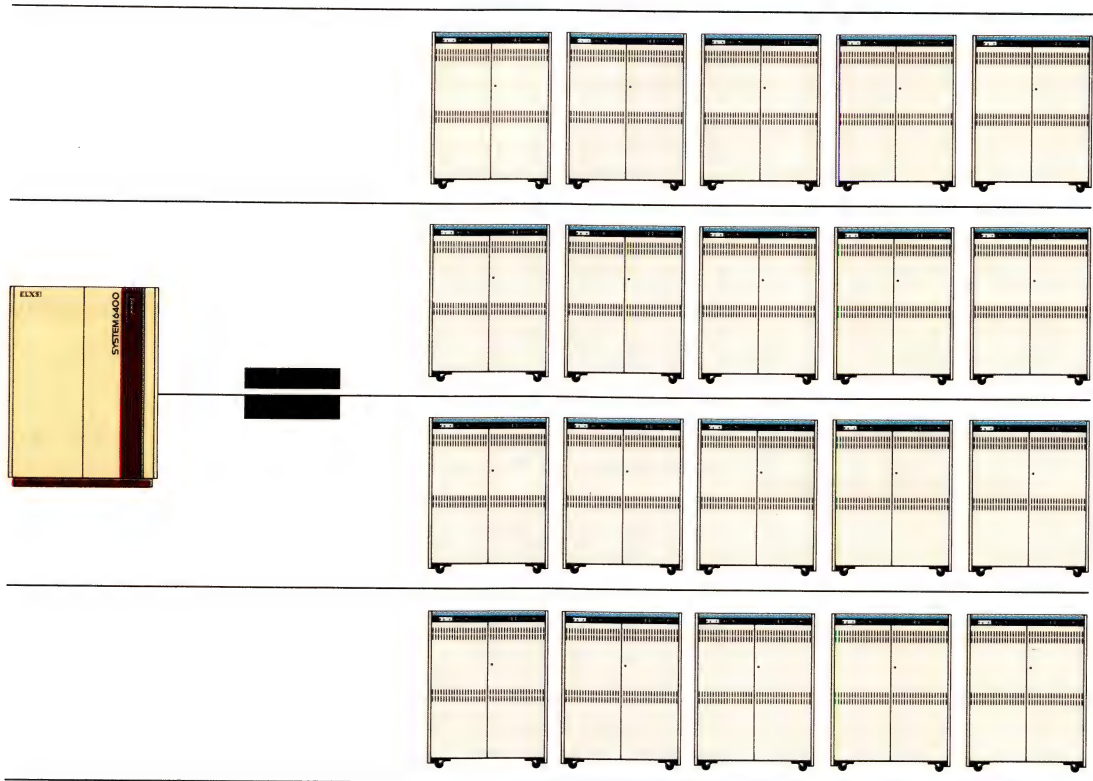
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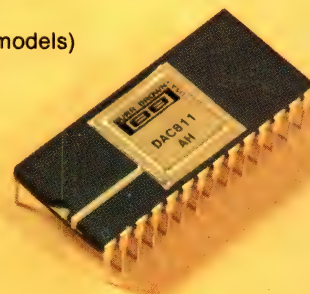
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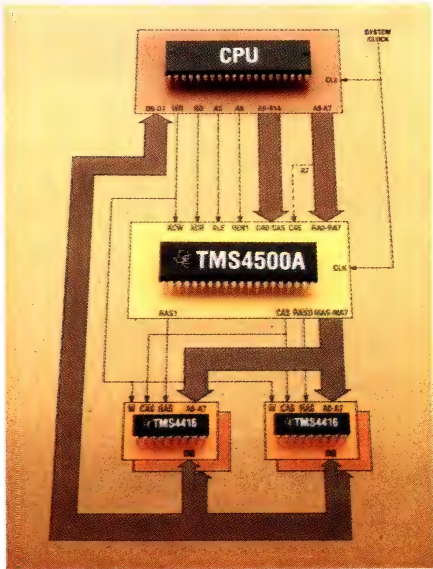
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# 16K x 4 DRAM cuts costs by 50% for Tektronix.



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## One TI chip links DRAMs with CPUs.

TI's TMS4500A DRAM controller saves design time and IC costs.

Easy to use, the TMS4500A supplies a reliable, single-chip interface between dynamic memory and the microprocessor.

The TMS4500A speeds and simplifies your design task by providing address multiplexing, cycle timing, arbitration logic, and refreshing—all on one chip. It saves substantial design time, circuitry, board space, and power. Plus replaces as many as 15 discrete support ICs.

Highly versatile, the TMS4500A interfaces with all popular microprocessors. And is compatible with DRAMs from 4K up—from any manufacturer.

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Using the TMS4500A, you can easily handle up to 256K bytes per controller with TMS4416s or TMS4164s. With additional decodes, you can go to 512K bytes and more.

## TI's 64K DRAM chip carrier: More memory in less space.

TI's 64K x 1 DRAM, the TMS4164, comes in a unique plastic chip carrier that lets you pack even more memory into less space.

### Dramatic reductions in board size

TI's low-cost 64K DRAM chip carrier provides twice the density of the conventional DIP. System size can be substantially reduced. And significant cost savings realized.

Unlike conventional DIPs, TI's advanced TMS4164 chip carriers can be surface mounted. As a result, the number of layers in the printed-circuit board is greatly reduced, and fewer boards are required.

### Ideal for SIPs

TI's 0.285-in. x 0.425-in. surface-mounted chip carriers are designed to meet the critical height requirements of single-in-line packages (SIPs), as well as offer the necessary low power dissipation. And TI now has in development single-in-line module arrays to meet your future system needs.

So when you need 64K DRAMs, rely on TI's outstanding choices. The TMS4164 for high speed, low power . . . and chip carrier packaging. The TMS4416 for high bandwidth and modularity. Both are cost-efficient. Easy to design with. And state of the art.

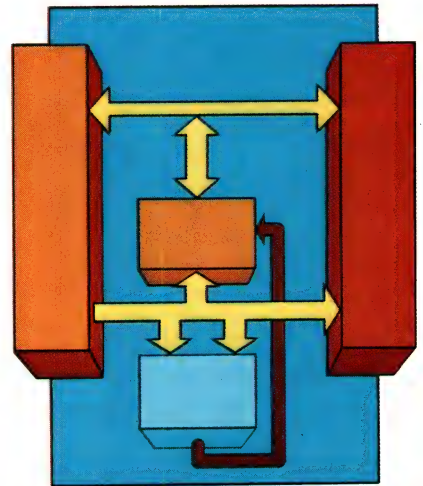
## New cache-tag comparator speeds system throughput.

TI's new TMS2150 cache address comparator can improve high-performance microprocessor or bit-slice system throughput by up to three times. Plus reduce cache memory IC count, board area, power dissipation, and cost.

With the TMS2150, no wait states need to be implemented in microprocessor access cycles in response to

slower cycling DRAMs. The TMS2150, in combination with high-speed static RAMs, completes an entire high-performance cache memory system. With a maximum 45-ns delay from address to match valid, the TMS2150 can provide TTL performance at one-tenth the parts count and 10% of the power.

Operating from a single +5-V power supply, the TMS2150 consists of a high-speed 512 x 9 static RAM array, parity generator and checker, and a 9-bit high-speed comparator.



High-speed cache memory systems utilizing the TMS2150 will enable high-performance microprocessors to set new cost-performance standards with large, low-cost dynamic main memory.

For more information on TI's high-quality 64K DRAMs, DRAM controller, cache-tag comparator, and plastic chip carrier, call the authorized TI distributor nearest you. Or contact Texas Instruments Incorporated, Dept. SMB023EC, P.O. Box 809066, Dallas, TX 75240.

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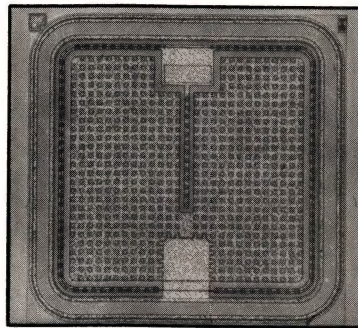
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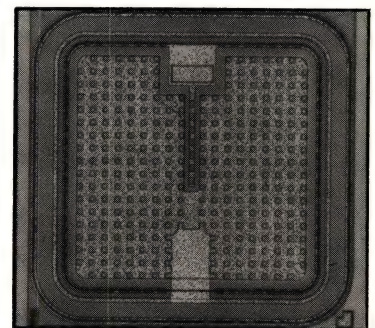
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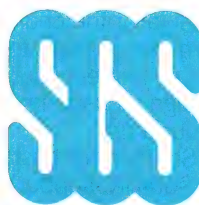
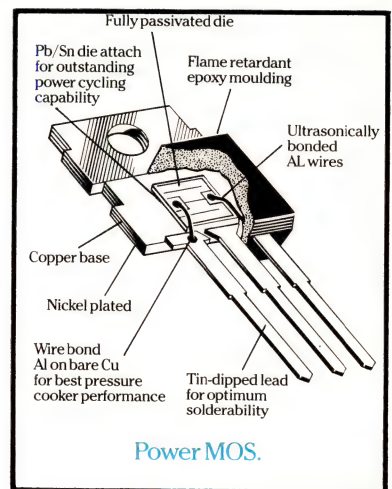
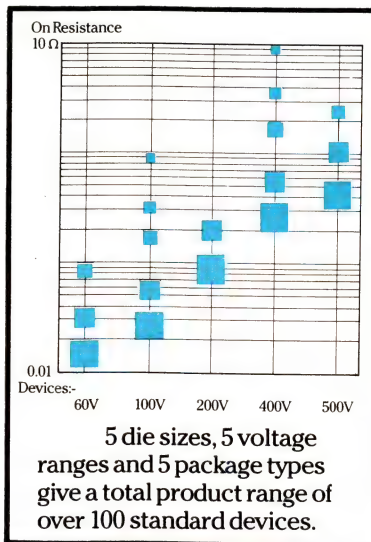
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## New products

Powerful microcomputers and a bevy of peripherals stand out from the crowd as a healthy industry displays its wares at National Computer Conference

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### Microcomputer makes use of Multibus II to mix multiple processors and operating systems in one box

One of the first companies to unveil a Multibus-II-based computer is using Intel's 32-bit parallel bus to form a new concurrent-processing architecture. Dubbed Tarch, it will eventually support a mixture of 16- and 32-bit central processors as well as real-time operating systems—all inside the same cabinet.

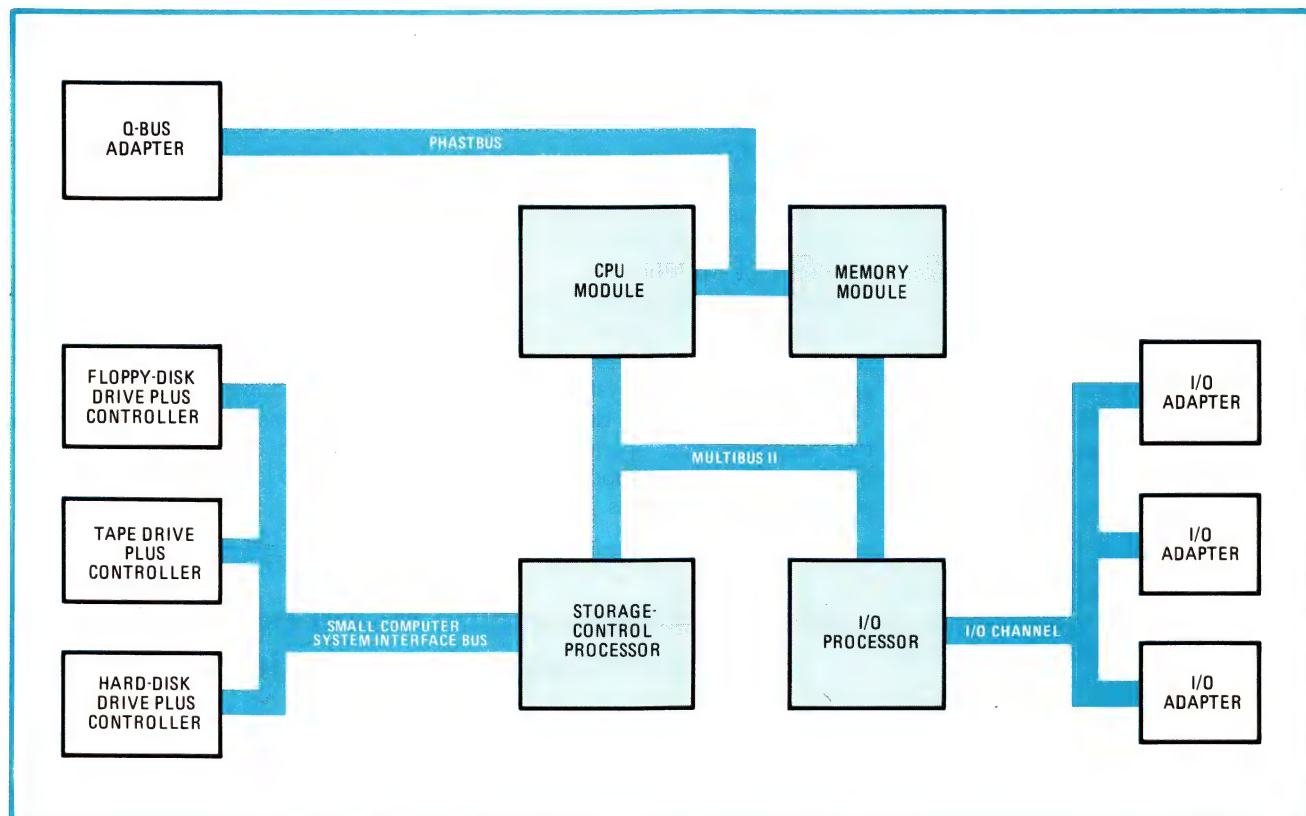
In July, Argonne Systems Inc., an 11-month-old start-up, plans to un-

veil the first wave of its Tarch-based multiple-coupled processors at the National Computer Conference, in Las Vegas, Nev. The first offering to original-equipment manufacturers is centered around a PDP-11-compatible 16-bit central-processing board based on a 15-MHz J-11 microprocessor from Digital Equipment Corp.

An SP3216 system configuration contains a single 16-bit central pro-

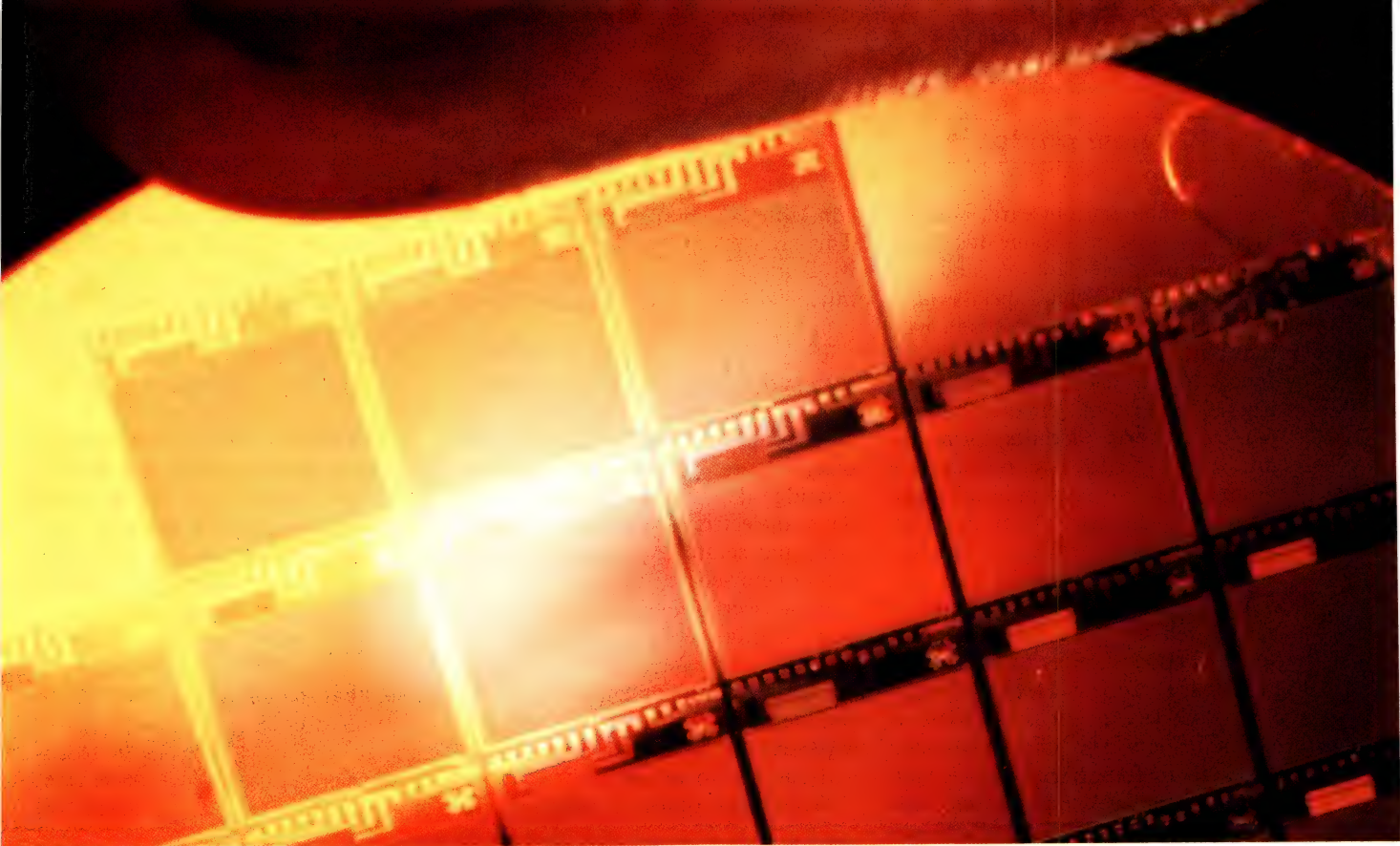
cessor unit. The MP3216 systems will have multiple CPU modules, each capable of running a different PDP-11-compatible operating system and of sharing common peripherals.

However, the Multibus-II-based Tarch concept is designed for full 32-bit processing. All memory subsystems and a high-speed cache are organized 32 bits wide. Later this year, Argonne is planning to introduce a



**Concurrent processing.** Developed to be microprocessor-independent, Argonne's Tarch architecture uses Multibus II. Initial versions of Tarch with CPUs will use processors from DEC and National Semiconductor, but boards based on chips from Intel and others will be added.





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## 16-K-byte buffer in 5¼-in. streaming tape drive smooths pauses and boosts data-transfer rates

A 5¼-in. streaming cartridge transport made by Kennedy Co. offers an unusual feature for this kind of peripheral: a 16-K-byte buffer memory that smooths the pauses that often occur when media are changed during backup operation. As a result, the Series 6500 has higher burst data-transfer rates and longer operation before repositioning than typical units, the company claims.

The transport incorporates another improvement as well: it ramps up to and from its 90-in./s speed in just 150 ms, so it can be repositioned in half the time that competing units need, the company says. Intended for Winchester disk-drive backup and data storage, the nine-track transport has two-track stepping heads with a formatted capacity of 60 megabytes

with a 600-ft cartridge and 45 megabytes with a 450-ft cartridge. Backup time for 60 megabytes requires about 12 min.

The Series 6500 comes in the full-height form factor with formatter card installed, as well as half-height without the formatter. The formatter, which has the QIC-02 drive interface standard, is compatible with the ANSC X3T9.6/83-20 interface and with the QIC-11 and QIC-24 tape formats for media interchangeability among transports. The drive-level interface is QIC-36.

The Kennedy tape drive employs self-clocking group-code recording with a recording density of 8-Kb/in. and 10,000 flux-reversals/in. Burst data transfer rate is 2 megabytes/s, while sustained data transfer is 720

Kb/s. A brushless, direct-drive capstan motor eliminates the troublesome belts found in conventional transports, while reducing instantaneous speed variation to within 1%, excluding the cartridge. Writing, reading, and rewind speeds are 90 in./s. The drive's envelope is equivalent to a half-height 5¼-in. drive, with the interface occupying equal space.

The drive weighs 3 lb and measures 5¾ by 1½ by 8 in. With the formatter, it is 3¼ in. high. Power requirements are +5 v dc at 2 A for the formatted version and 1 A without formatter. The brushless dc capstan motor requires 12 v dc at 0.5 A while operating and 1 A during start-up. Data reliability is 1 in 10<sup>8</sup> bits for soft errors and 1 in 10<sup>10</sup> bits for hard errors. The mean time between failures is said to be 5,000 h, mean time to repair to be 30 min.

In single-unit quantities, the Series 6500 is \$1,275 with the formatter and \$875 without it. Evaluation units

### The MT8950 Data Codec

interfaces slow speed data at up to 19.2 Kbps (e.g. RS232) to a 64 Kbps TDM channel format (ST-BUS).

### The MT8964/65 PCM Filter/Codecs

perform A/D conversion in either A-Law or  $\mu$ -Law. Available in 18 pin DIPs, these ICs offer advanced system control capabilities for PABX and wider applications.

### The MT8980/81 Digital Time/Space Switch ICs

are non-blocking matrices that switch PCM encoded voice and/or data at 64 Kbps/channel. The MT8980 matrix is 256 × 256

channels and the MT8981 matrix is 128 × 128. Both ICs are in 40 pin DIPs.

### The MH89700 Digital Line Interface Module

performs full-duplex digital line interfacing at 256 Kbps over 2-pair common telephone cable. It offers user access via an 8-bit parallel I/O interface or by the ST-BUS, and is compatible with 6800 and 68000 microprocessor series.

### The MH89750 T1 Digital Trunk Interface Module

performs 2-way conversion between the T1 digital trunk format (1,544 Mbps) and the ST-BUS format.

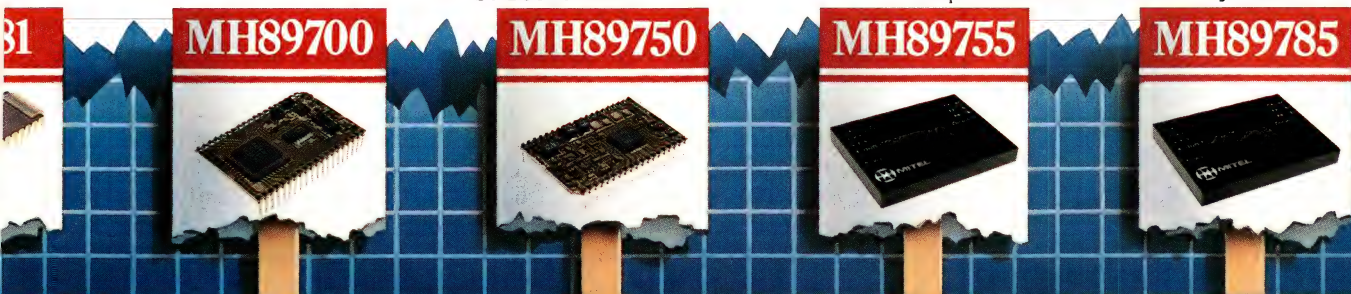
### The MH89755\* T1 Digital Trunk Interface Module

has all the power of the MH89750 with the addition of a high speed, 8-bit parallel I/O.

### The MH89785\* CCITT Digital Trunk Interface Module

performs 2-way conversion between the CCITT digital trunk format and the ST-BUS format or a high speed 8-bit parallel I/O.

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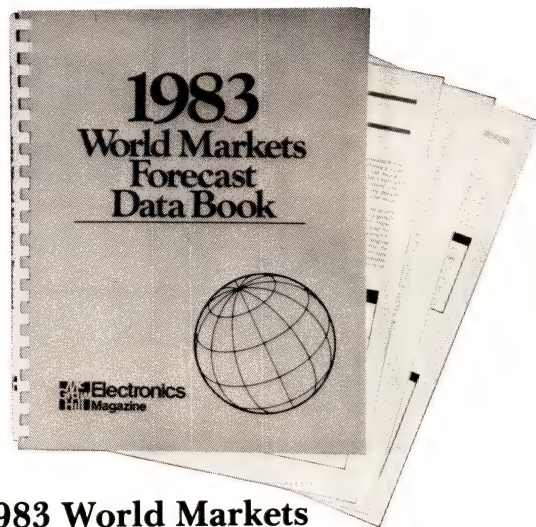
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EL 1





# Inexpensive design system uses icons

Work station uses two pc boards for electronics to pack complete system, including hard- and floppy-disk drives, inside just one desktop cabinet

by J. Robert Lineback, Dallas bureau

What is good for office workers appears to be even better for systems designers, especially if it is an object-oriented user interface on desktop computers. That is the thought behind a new engineering work station from Cadnetix Corp., which moves its unique icon-and-mouse-driven interface into printed-circuit-board-design markets. The CDX-9000 is slated for introduction at this week's Design Automation Conference, in Albuquerque, N. M.

Based on a 68010 microprocessor and containing 35 megabytes of storage on a Winchester disk, the tabletop computer-aided-engineering unit and CAE software have been tailored to help system designers manage projects. Cadnetix believes it has greatly cut the cost of CAE work stations by laying out the 9000's electronics on two pc boards and by packaging a Winchester disk drive and a 5¼-in. floppy-disk drive in a desktop cabinet together with a 17-in. monochrome bit-map monitor.

The basic model, which sells for \$36,500 in quantities of four to nine, includes a 10-MHz 68010 with memory management, 1 megabyte of random-access memory (expandable to 3.5 megabytes), a 35-megabyte Winchester, an 814-K-byte (formatted) 5¼-in. floppy-disk drive, a three-button electronic mouse, a detachable keyboard, and a monochrome monitor with a resolution of 1,024 by 800 picture elements. A second model, the CDX-9100, sells for \$27,500 in quantities of four to nine and has 0.75 megabyte of RAM and an 18-megabyte Winchester. An optional Ethernet interface is also available.

The CDX-9000 CAE computer runs Cadat logic and fault-simulation

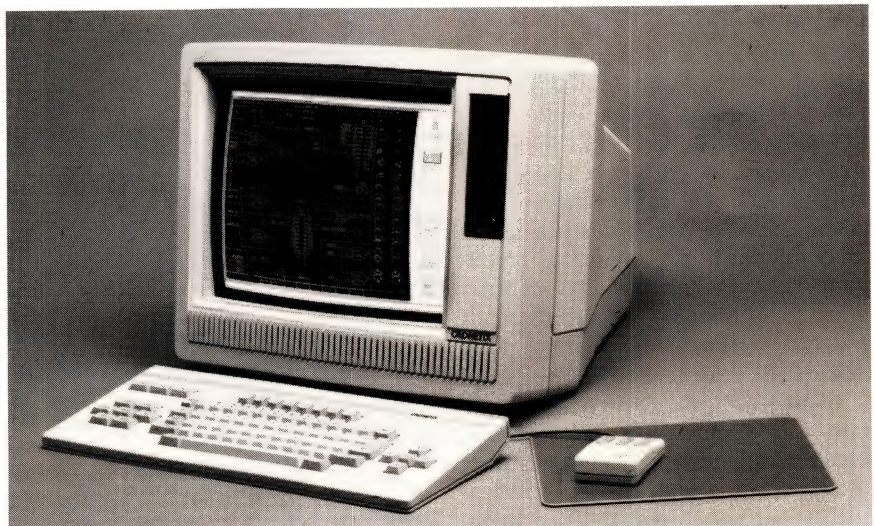
packages, which have been licensed from HHB Softron Inc., of Mahwah, N. J. Cadnetix has reworked the Cadat software interfaces to run on its object-oriented operating system. In addition, a multicolor CAE work station called the CDX-9000c, available with a 19-in. monitor, costs \$55,000 each in quantities of four to nine. Like the company's existing CDX-5000 system [*Electronics*, Feb. 24, 1983, p. 159] for pc-board layout, the color unit has an additional pedestal cabinet to house the electronics.

The 9000 taps directly into a relational data base, which can reside on an Ethernet local network and be shared by a CDX-5000 color-layout work station. By tightly linking the data base to both the conceptual phase of pc-board design and physical layout, Cadnetix believes that its CAE system can dramatically shorten product-development cycles, reduce errors, and aid project management.

For instance, layout engineers working on the CDX-5000 automati-

cally pass information back to designers through the shared data base. This process annotates product documentation for checking by designers and use in production, parts buying, field service, and product literature. Both the new CDX-9000 CAE computer and the CDX-5000 layout station run under the company's proprietary object-oriented multiwindow operating system. When an engineer turns on the station, the operating system creates a work surface with a number of icons—graphic objects that symbolically represent file cabinets, folders, a clock, a printer, a plotter, magnetic tape, and the like.

**Mouse.** As in Apple Computer Inc.'s Lisa and Macintosh, the user enters commands into the computer by using a mouse to position the cursor atop an icon. Once selected, directories, files, and diagrams pop up over the work surface on the bit-map display. "One of the important things about this user interface is that it allows you to take six months



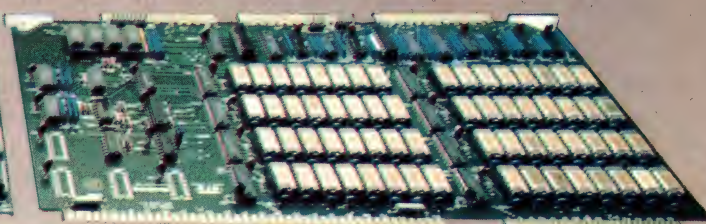
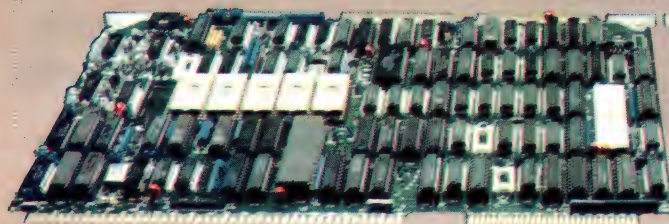
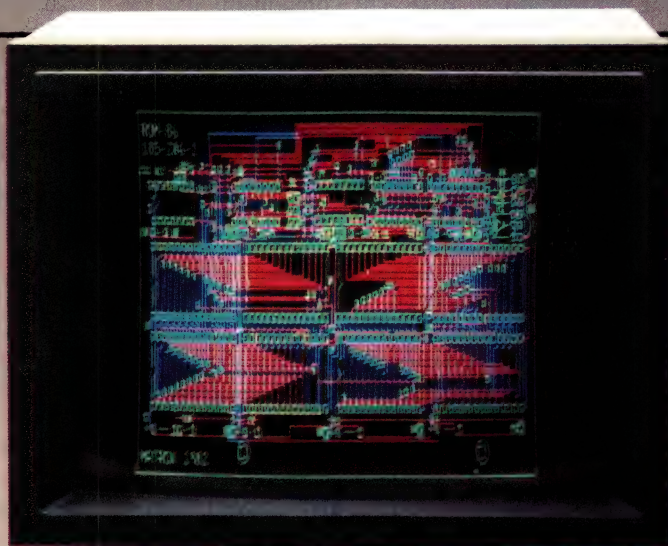


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**DISPLAY RESOLUTION:** 1024 x 768 pixels non-interlaced at 60Hz or up to 1600 x 1200 pixels interlaced at 30Hz

**READ/WRITE AREA:** 1024 x 1024 x 4 bits/pixel expandable to 1024 x 1024 x 16 or 2048 x 2048 x 4

**SPEED:** Four pipelined on-board processors draw graphics primitives at speeds of 50 to 800 nsec/pixel

**COLOR:** 16 display colors can be selected from a palette of 256 different shades

**SOFTWARE:** On-board 16 bit CPU with resident graphics software interprets over 256 commands and supports local segments, 2D primitives, tablet tracking, rubber banding, etc.

**MODULARITY:** GXB-1000 is fully Multibus compatible (IEEE-796), and operates from a single + 5V supply

Multibus - TM Intel \* QTY 100

The GXB-1000 is a complete color graphics display system implemented on two Multibus boards. The system executes a display file containing high level graphics commands, generated by the user's host CPU. The GXB-1000 includes all the necessary hardware and software to draw lines, polygons, circles, characters, etc.

The GXB-1000 represents true state of the art performance. The boards generate the highest display resolution available from a raster scan device. The multi-processor pipelined architecture provides the highest possible drawing speeds.

Over six man years of Matrox programming effort have gone into the development of the on-board graphics software. An extensive command set allows the user to construct complex images with a minimal number of host CPU instructions and time.

The unmatched performance and low cost of GXB-1000 make it the perfect solution for OEM color graphic displays. Additionally, Matrox can provide RGB monitors, CPU boards, memory boards, cardcages and keyboards for complete display system requirements.



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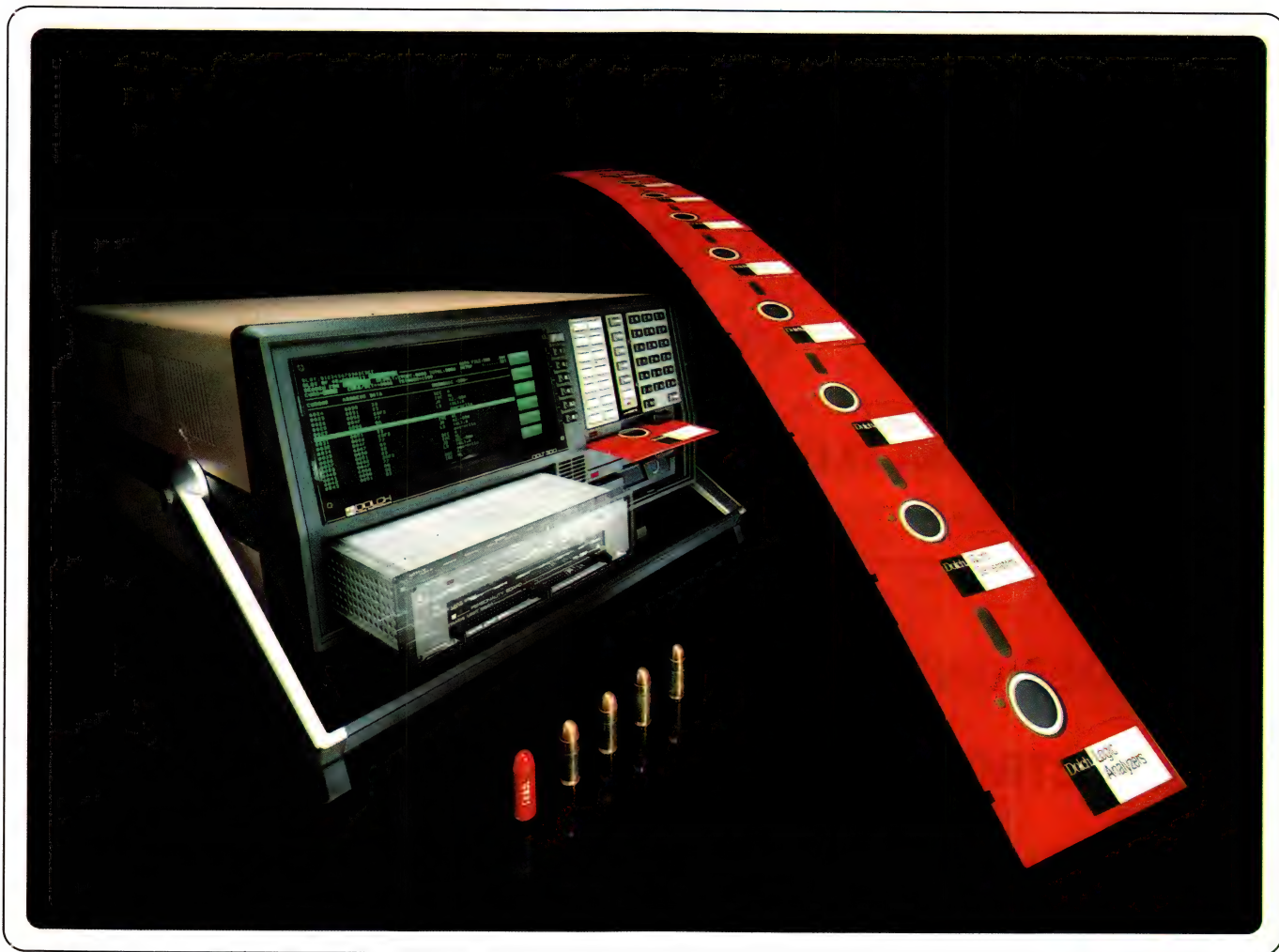
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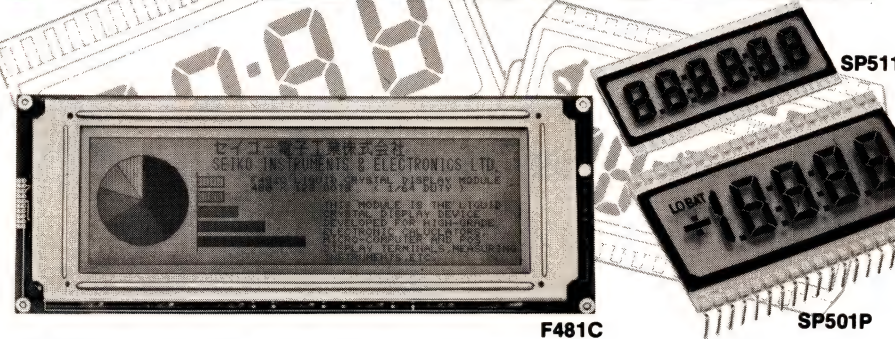
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|------------|--------------------------------|-------------------|------------------------------|---------------------|------------------------------------------|------------------|
| M3214      | 210×80×12.1                    | 152×40            | 32 Characters×4 Lines        | 3.50×5.15           | 6.5V                                     | Serial           |
| M4012      | 186×32.8×9.4                   | 147.4×16          | 40 Characters×2 Lines        | 2.65×3.75           | 5.0V                                     | Parallel         |
| M8011      | 260×42.5×9.4                   | 220×18            | 80 Characters×1 Line         | 2.25×3.46           | 5.0V                                     | Parallel         |
| F1632      | 210×80×12.1                    | 152×40            | Full Dots                    | Full Dots           | 6.5V                                     | Serial           |
| F2416      | 220×80×12.7                    | 160×53            | Full Dots                    | Full Dots           | 5.0V                                     | —                |
| F4816      | 270×70×12.7                    | 225×44            | Full Dots                    | Full Dots           | 5.0V                                     | —                |
| F481C      | 290×110×12.9                   | 225×74            | Full Dots                    | Full Dots           | 5.0V                                     | —                |

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|--------------|------------------------|-----------------|------------------|--------------------|------------------|
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| SP521P/SP521 | 50.80 30.48            | 1.10            | 45.72 17.78      | 7.00 12.70         | 3 1/2            |
| SP532P/SP532 | 69.85 30.48            | 1.10            | 64.77 17.78      | 6.60 12.70         | 6                |
| SP535P/SP535 | 93.85 30.48            | 1.10            | 88.77 17.78      | 6.60 12.70         | 8                |
| SP538P/SP538 | 81.28 38.10            | 1.10            | 76.20 25.40      | 9.14 17.78         | 5                |

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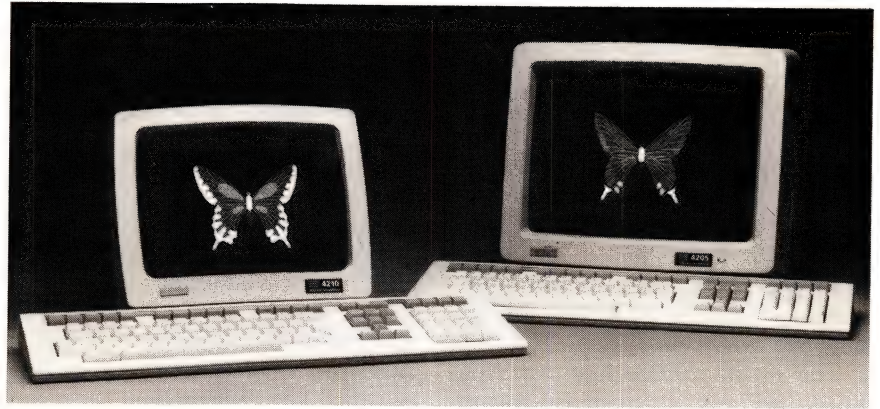


### Computer graphics

## Dual processors let displays draw pixels fast

Based on a dual-processor architecture, the HiScan line of graphics displays achieves graphing speeds of 1 million pixels/s. The systems employ a proprietary complementary-MOS graphics processor that works in conjunction with a Z8002 16-bit microprocessor.

The 4210 monochrome display has a resolution of 800 by 600 pixels, while the 4205 color model has a 600-by-300-pixel resolution. The non-interlaced terminals support 80- and 132-column formats, with characters formed on a 10-by-20-dot matrix. Using two memory planes, the monochrome model offers a four-level



el gray scale. The color terminal uses four planes and simultaneously displays 16 colors out of a palette of 64.

The displays are based on Digital Equipment Corp.'s VT200 terminals. Compatible with many terminal protocols, the 4210 and 4105 units provide Tektronix' 4027 or 4105 or DEC's Regis graphics protocols and standard DEC VT220 text and TEK 4010/4014 graphics functions.

Text features include a setup menu displayed in English, French, or German and 132 column modes, downloadable character fonts, and 15 programmable function keys.

Scheduled to be available in July, the model 4210 will be priced at \$2,195, the 4205 at \$2,995.

Digital Engineering Inc., 630 Bercut Dr., Sacramento, Calif. 95814. Phone (916) 447-7600 [Circle reader service number 361]

### Geometry terminals produce 3-d frame and solid models

Two additions to the 2020 line of three-dimensional geometry-processing terminals, the models 7115 and 7215, address applications in the design, analysis, and drafting of outline and solid models. All models in the series can perform the same functions locally, including data-base management; 3-d geometry transformations; high-speed drawing of vectors, polygons, and shaded surfaces; and communications with a host computer.

Model 7115 draws at speeds of up to 40,000 vectors/s. Model 7215 achieves 660,000 vectors/s and uses static random-access memory and a proprietary bit-slice drawing processor to accelerate vector setup time. Both models are configured with the company's raster processor, a proprietary emitter-coupled-logic design for writing vectors in raster-scan format to refresh memory, and a MC68000 processor for communications, data-base management, and geometry processing.

Each model includes a 19-in.-diagonal, 60-Hz, color cathode-ray-tube terminal with 1,280 by 1,024 pixels and 768-K bytes of memory.

Available in 90 days, models 7115 and 7215 are priced at \$28,000 and \$44,000, respectively.

Ramtek Corp., 2211 Lawson Lane, Santa Clara, Calif. 95050. Phone (408) 988-2211

[Circle 362]

### Display builds images using two resolutions at once

The LEX 90 line of raster-scan display and graphics systems are fashioned to satisfy both the business and technological requirements of the system integrator. The LEX 90's basic display controller writes vectors at an average of 600 ns per picture element in any direction and fills the screen in 37.5 ns. For efficiency, the company's horizontal microcode processes multiple arithmetic and read/write instructions concurrently.

The LEX 90/35 model 2 is a graphics system featuring two software-selectable resolutions for gener-

ating shaded images and high-resolution drawings. The system allows the simultaneous display of both a 640-by-512-by-8-bit image and a 1,280-by-1,024-by-4-bit overlay. A true-color version is available, and a pseudo-color version can be used for applications needing higher resolutions.

The model 3 supports eight planes of a 1,280-by-1,024-pixel display memory at 60 Hz, noninterlaced. Also containing an 8-bit color look-up table, it works with 60- or 30-Hz monitors. Prices for the model 2 range from \$13,925, for the four-plane configuration, to \$22,925, for the true-color system. Model 3 costs \$19,850 for the eight-plane configuration. Deliveries take 120 days.

Lexidata Corp., 755 Middlesex Tpke., Billerica, Mass. 01865. Phone (617) 663-8550

[Circle 363]

### Bit-mapped terminal addresses 2,048 by 2,048 points

With a bit map of 2,048 by 2,048 addressable points, the model 2000A is a graphics terminal that facilitates



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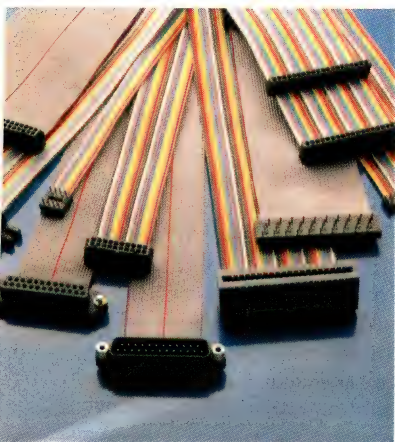
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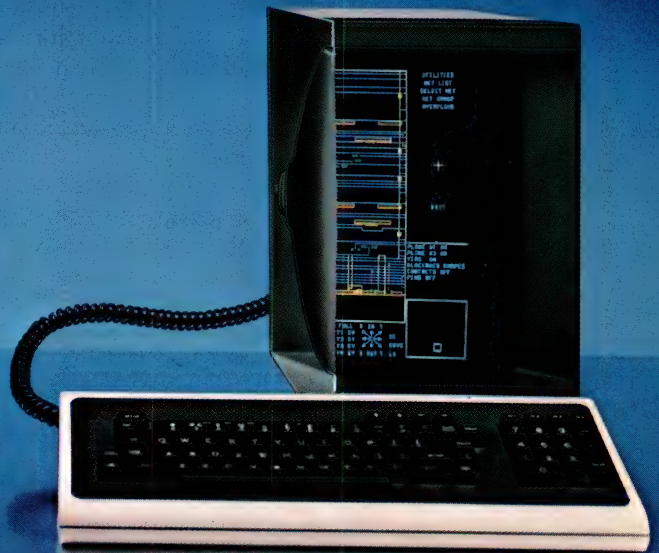
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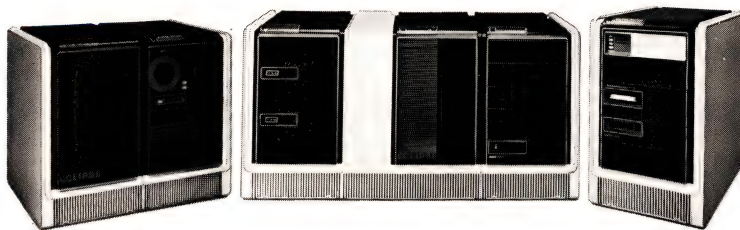


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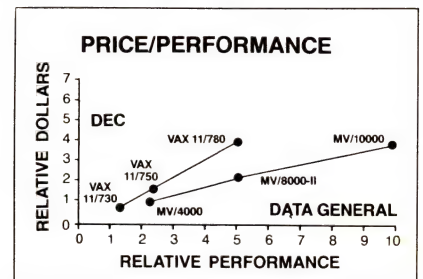
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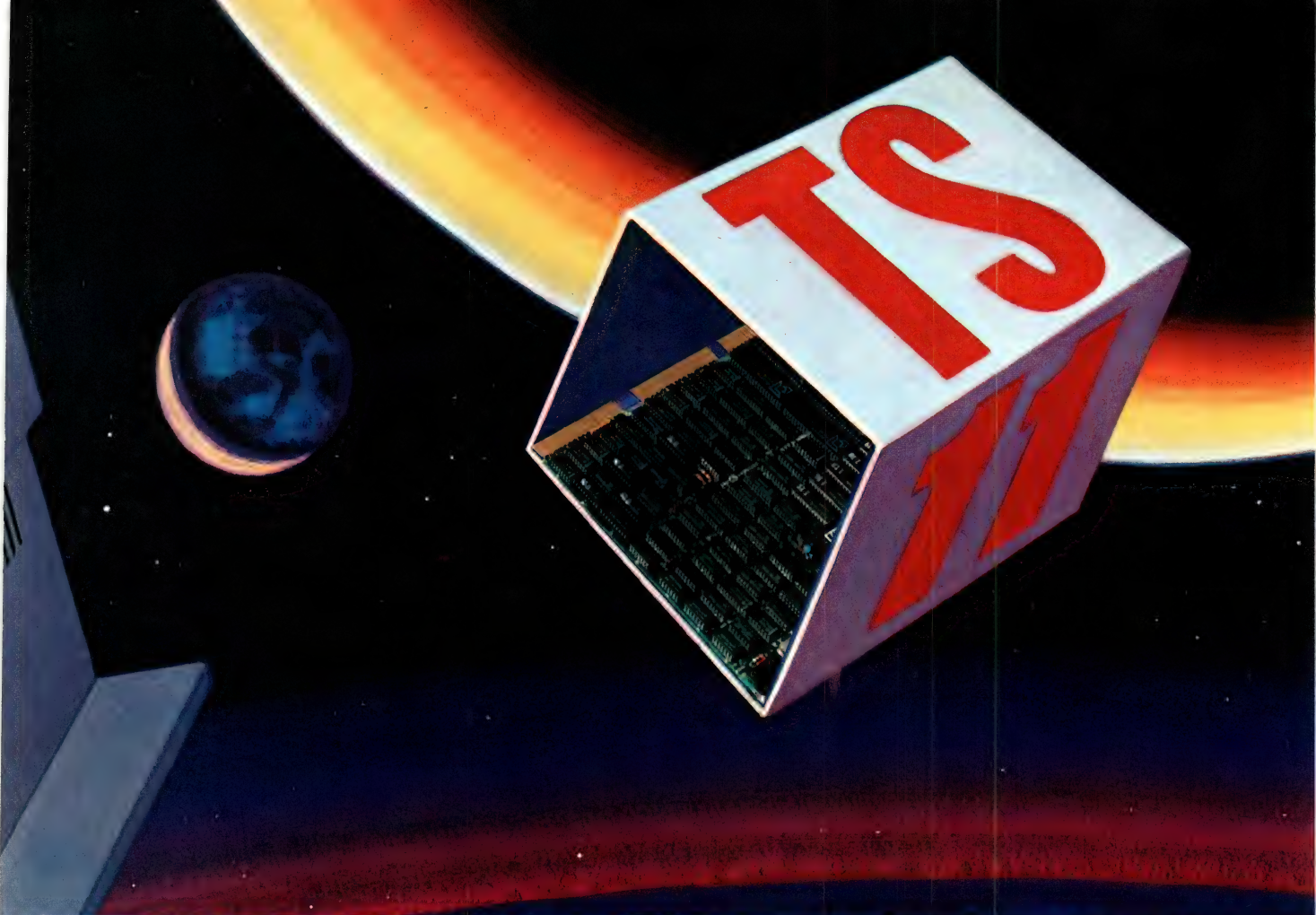
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## Software

auxiliary equations and substitutes the reduced auxiliary expression for each occurrence in subsequent equations. It also allows 400 output variables and equations and as many as 111 driving variables, which are either input or output variables used within the logic net.

The program is available now (for VAX systems running the VMS operating system) at a price of \$1,895, and in C source form for \$9,000. A less powerful version, for use on IBM Corp. Personal Computers running MS-DOS and the Osborne-1 under CP/M, is available in executable form for \$595, and in C source form for \$5,000.

Mirashanta, 2008 Deerpark Pl., #350, Fullerton, Calif. 92631. Phone (714) 996-4877

[Circle 415]

## Language helps researchers of artificial intelligence

A programming language called Domain Lisp increases the application capabilities of the Domain system, helping to improve the productivity of those working in artificial-intelligence research. It features a high level of integration within the company's language family, giving the application programmer the use of multiple languages.

Lisp is available on all the firm's systems, including the DN300, the DN320 with floating-point hardware, and the DN460 and color-DN660 work stations. Included is an interpreter for quick checkout or prototyping and an optimizing compiler for the creation of fast production applications. Available in 60 days, the product costs \$1,850 per node.

Apollo Computer Inc., 15 Elizabeth Dr., Chelmsford, Mass. 01824. Phone (617) 256-6600

[Circle 417]

## Package uses host's resources to manage code development

A software development and management system called SourceTools uses the resources of a mainframe

computer to build application code and manage the development process, thereby reducing the project's complexity. It supports cross-development software projects.

SourceTools can be used with a package written in any language and with any standard text file. The system employs three packages that together manage software projects. One contains four programs to control the creation and modification of source codes. The second automatically keeps programs up to date as their components change. The third, two programs working together, eases the task of maintaining parallel source files on different systems.

SourceTools is available now and is priced at \$4,500 for the RSX operating system and the VMS operating system running in the RSX compatibility mode, and \$3,600 for the RSTS operating system.

Oregon Software Inc., 2340 S.W. Canyon Rd., Portland, Ore. 97201. Phone (503) 226-7760

[Circle 416]

## CAD software creates rf, microwave circuits

Touchstone, a computer-aided-design software package that creates radio-frequency and microwave circuits, runs on a wide range of microcomputers, including the IBM Corp. Personal Computer. To run Touchstone, the computer must incorporate the 8087 math coprocessor, have 512-K bytes of random-access memory, and run PC-DOS or MS-DOS.

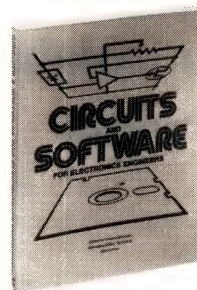
Touchstone includes an interactive language that will modify the layout of a model it has designed. Then, the CAD product performs another analysis to make sure the original parameters are intact. The company will offer ongoing technical support and updated catalogs of element models, such as microstrip lines, transmission lines, and S-parameters.

The product will be available in October at a price of \$7,500 per copy. Five copies will cost \$29,200. EEsof Inc., 5743 Corsa Ave., Suite 216, Westlake Village, Calif. 91302. Phone (818) 991-7530

[Circle 418]

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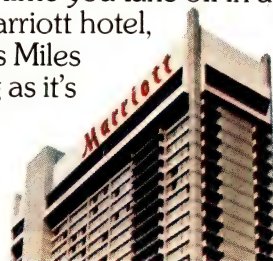


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## New products/materials

A laminate called BEND/flex is designed for nonflexing applications where the installed circuitry will exist in more than one plane. The copper-clad, epoxy circuit material can be drilled, routed, blanked, or wave-soldered in both single- and double-sided plated-through-hole configurations. The boards have been found rigid enough to support components while retaining true formability. Available now in thicknesses between 0.015 in. and 0.030 in., the installed cost for the BEND/flex circuitry is estimated to be about \$3.

Rogers Corp., 2001 W. Williams Field Rd., P. O. Box 700, Chandler, Ariz. 85224. Phone (602) 963-4584 [Circle reader service number 401]

A conductive silver ink for printed-circuit boards allows conductive circuit fabrication without the normal processing. The silk-screenable ink can be soldered and adheres after low-temperature curing. The CBS-1709 material can be used on any pc board unable to withstand a processing temperature over 145°C. The ink, which has a resistance of less than 100 mΩ/square can be soldered with silver-bearing solders. The CBS-1709 ink is priced at 40¢ to 42¢/g in large quantities and is available in two weeks.

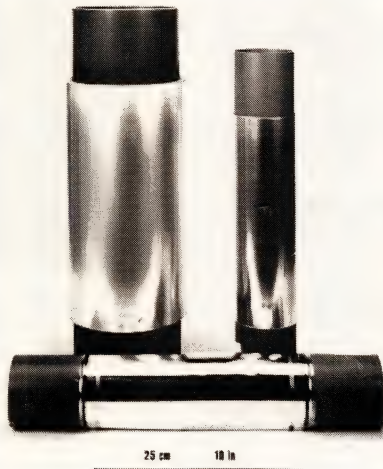
International Microelectronics Research Corp., 4951 E. 29th St., Tucson, Ariz. 85711. Phone (602) 747-3918 [Circle 402]

**Produced in copper alloys** and Alloy 42, a series of stamped 48-pin leadframes for plastic dual in-line packages are supplied in strips of six with a pitch of 1.040 in. and a width of 2.660 in. Options include a choice of two pad sizes and spot plating with gold or silver. Available now, 1,000 Alloy 42 leadframes cost \$97.50, compared with \$72 for copper.

Koltron Corp., 1380 Bordeaux Dr., Sunnyvale, Calif. 94086. Phone (408) 734-0070 [Circle 403]

**Biaxially oriented films** can replace ceramics in large-surface piezoelectric applications. The line of films features polyvinylidene fluoride substrates that are fabricated to generate voltage when deformed or to change

shape when subjected to an electrical field. Providing acoustic impedance close to that of water, the films come in metalized or nonmetalized form in thicknesses of up to 40 μm on rolls up to 25 cm wide or in 15-by-25-cm sheets. Applications include acoustics, ultrasonic sensors, vibration generators, and medical sensing units. Available now, the films are priced



at from \$20/ft<sup>2</sup> and up, depending on the configuration.

The Solvay American Corp., 609 Fifth Ave., New York, N. Y. 10017. Phone (212) 838-8563 [Circle 404]

**A silicone elastomeric foam** is designed for insulation and vibration damping of electronic components such as printed-circuit boards and wiring. Designated RTF-760, the two-component material offers a fast cure, is noncorrosive and flame-retardant, and does not interfere with electrical systems.

The foam has a density of 15 lb/ft<sup>3</sup> and a temperature resistance of -60°F to 400°F, thus remaining elastomeric over a broad temperature range. The foam has a 25% compression deflection of 5 lb/in.<sup>2</sup> as well as a compression of 10% to 15% after 22 h at 73°C, which allows it to return to its original shape after a load is removed. Priced competitively with silicone foam, the material is available now.

General Electric Co., Silicone Products division, Waterford, N. Y. 12188. (518) 266-3544 [Circle 406]

**Three glass-filled grades** of a Radel A-400 resin will withstand the 550°F temperatures that can be encountered in wave-soldering electrical connectors and printed-circuit boards, the firm says. Radel A-400 has a heat-distortion temperature of 205°C and an anticipated 180°C Underwriters' Laboratories continuous rating. The grades, Radel AG-410, 420, and 430, contain 10%, 20%, and 30% glass loadings, respectively.

The compounds offer a range of rigidity, tensile strength, and heat-deflection temperatures. Available now, the compounds are priced at about \$4.25/lb in truckloads.

Union Carbide Corp., Dept. M1523, Old Ridgebury Rd., Danbury, Conn. 06817

[Circle 407]

**Two adhesives** for staking surface-mounted devices to printed-circuit boards before soldering can be applied by such methods as pneumatic applicators. Designated the 930-12-4 and 990-30-7, the adhesives are single-component, solventless materials meeting a range of requirements for application and cure techniques. The 930 material, which can cure with heat in less than 15 min at 100°C, was developed for pin-transfer-application equipment. The 990 material can cure within 15 s. Available within three weeks, the 930 material is priced at \$82/quart in 21-to-100-qt orders. The 990 costs \$120.50/qt in 21-to-50-qt orders.

Amicon Corp., 25 Hartwell Ave., Lexington, Mass. 02173. Phone (617) 861-9600

[Circle 408]

**Providing rapid bonding**, the 600 series of structural curing adhesives are intended for use in structural wire tacking, chip bonding, conformal coating, and the manufacture and repair of printed-circuit boards. The aerobic acrylic adhesives cure after exposure to ultraviolet light and have resistance to temperatures ranging from -65°F to 450°F and a tensile strength of 3,000 lb/in.<sup>2</sup> Priced from \$30 to \$60, depending on the quantity, the adhesives are available now.

American Chemical & Engineering Co., 51 Greenwood Rd., Torrington, Conn. 06790. Phone (203) 482-1010 [Circle 409]



## Products newsletter

### **Flexible front end aids CAD/CAE software**

Silvar-Lisco has added a highly flexible interactive front end to its SL-2000 software for computer-aided design and engineering. **Version 5 of the Structured Design System includes a computer-aided schematic system (CASS) that makes it possible to enter logic designs on a graphics terminal interactively.** SDS consists of a set of programs providing schematic-design entry and checking, as well as hierarchical design transformation. With CASS, it creates a multiwindowing capability that automatically updates all windows to reflect changes made in any. The SL-2000 software operates with VAX, IBM 4300 and 3800, and Prime computers, and with the Apollo work station. With CASS, it is priced at \$14,000 for the Apollo version and \$30,000 for the others. It will be available in January.

### **Computer board can hold 128-K bytes of EE-PROM**

Based on the 16-bit iAPX-186 microprocessor, a single-board computer from Monolithic Systems Corp. of Englewood, Colo., costs \$2,280 with 128-K bytes of on-board dynamic random-access memory. **The MSC 8186 module can accommodate up to 512-K bytes of RAM and features sockets for 128-K bytes of erasable programmable read-only memory.** It also offers 24-bit addressing, eight levels of interrupts (expandable to 64), and serial input/output. Master arbitration logic permits up to three bus masters to share the same bus in a serial priority setup or up to 16 bus masters employing an external parallel priority networking scheme.

### **100-kilobaud modem works on 5,000-ft lines**

A short-haul (up to 5,000 ft) RS-232-C-compatible interface unit is intended for dedicated asynchronous transmission at speeds of up to 100 kilobaud over twisted-pair wiring. Introduced by CBM Electronics Inc., Costa Mesa, Calif., **the TE-5000 modem is suited for in-plant or localized uses, simplex or full-duplex transmission.** Optical couplers reduce electrical interference picked up along the transmission line. The 2-lb unit is priced at \$139.

### **Broadband GaAs FET operates in 20-GHz range**

A new broadband gallium arsenide field-effect transistor that operates in the 20-GHz range is available from Hughes Aircraft Co.'s Microwave Products division, Torrance, Calif. Designated the CO311H-2000, it is guaranteed to work in a 50- $\Omega$  system over a 2-GHz typical bandwidth. **It is intended as a medium-power driver with 6.5-dB gain guaranteed at a 100-mW output level.** Several of the devices can be combined with quadrature couplers to achieve higher power levels. Mounted on an internally matched chip-carrier, the FET is compatible with 25-mil alumina microstrip circuits and has 1-mil-thick gold leads.

### **32-bit work station has four planes of color**

Broadening its line of engineering work stations, Apollo Computer Inc. is introducing a 32-bit color-graphics unit that the Chelmsford, Mass., company says costs a quarter of what competing products do. **Based on Motorola's 68010 processor, the DN550 provides a multiwindow, multi-tasking environment that handles up to 24 concurrent processes with 16 megabytes of virtual address space each.** With four planes of color, a local-network interface, Apollo's Aegis operating system, and 1 megabyte of memory, the DN550 lists for \$31,500 and requires four months for delivery.



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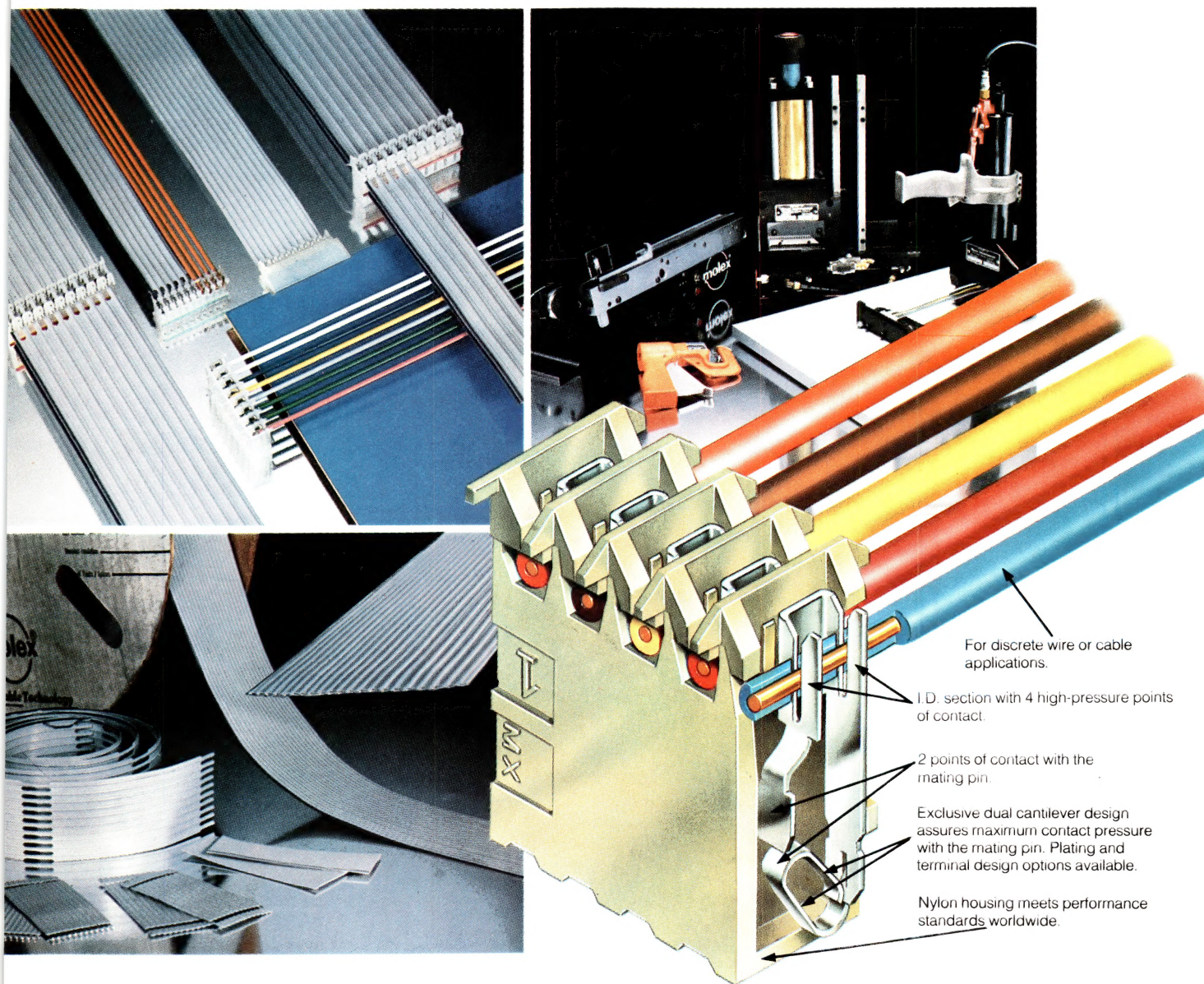
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